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LIQUID CRYSTAL AIRBORNE DISPLAY

HUGHES AIRCRAFT COMPANY
CENTINELA AND TEALE STREETS
CULVER CITY, CALIFORNIA 90230

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Final Report for Period March, 1973 – December, 1976

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J. O. Mysing, Project Engineer
Information Presentation and Control Group
System Technology Branch

FOR THE COMMANDER

H. Mark Grove
Chief, System Avionics Division
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A solid-state liquid crystal television display panel is described. This display has been developed as a replacement for the cathode-ray tube in direct-view and head-up display applications for tactical aircraft. Its key advantages are: (1) high contrast in small and large areas, (2) gray shade capability under all levels of illumination including direct-sunlight, (3) uniform high resolution over the entire display area, (4) interface similar to CRT TV display and (5) low power, weight, volume.

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Cockpit installations have been designed for the display which permit viewing under day and night conditions. Measurements have confirmed that the display brightness and contrast remain superior to the CRT for all single-place cockpit viewing positions under anticipated in-flight illumination conditions. The presentation of gray scale television images under direct sunlight illumination has been demonstrated.

The display is built using silicon LSI circuit technology to form the metal-oxide semiconductor addressing circuits which define a matrix of electrodes used to directly activate a liquid crystal film. The present display is 2" x 2" square and consists of 40,000 elements arranged in a 200 x 200 array.

Techniques have been successfully illustrated for increasing the size of the display by assembling a mosaic array of modules, that are electrically interconnected.

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PREFACE

This report covers work performed under the auspices of the Research and Technology Division of the Air Force Avionics Laboratory at Wright-Patterson Air Force base. The work was initiated in March of 1973 as a program to develop an advanced synthetic array radar display under the direction of contract monitor Mr. A. S. Jahren (AFAL/NVL). Later the foal of the program was broadened to provide for the development of a liquid crystal airborne display, and the responsibility for the program was transferred to contract monitor John O. Mysing (AFAL/AAM). Still later, in March 1976, the task was expanded to include an investigation of liquid crystal mosaic array display assembly techniques with funding provided by NASA through the Air Force. That additional work was monitored for NASA by Dr. Roger Breckenridge of the NASA Langley Research Center.

The work covered herein was performed by the Display Systems and Human Factors Department, Engineering Division, Radar Systems Group, of Hughes Aircraft Company in Culver City, with the assistance of the Hughes Research Laboratories at Malibu, the Hughes Semiconductor Research Laboratories at Newport Beach, The Hughes Component and Materials Laboratories at Culver City, the Microelectronics Technology Department at Fullerton, and the Hughes Industrial Products Division at Carlsbad. Special acknowledgement is gratefully made to the following for contributions to the performance of this effort: Messrs. William C. Hoffman and Richard N. Winner for their administrative aid as program managers; Dr. Hans Dill, Dr. Ronald Finnila, Dr. Alex Leupp, Dr. Lewis Lipton, Dr. Denis McGreivy, Dr. Henry T. Peterson, Dr. Thomas Toombs, and Craig Stephens for semiconductor device development; William R. Byles for performance measurements and analysis; Joseph B. Setto and Harold V. Magnuson for display package design; James C. Rill for array assembly technique development, and Dr. Hong-Sup Lim, Dr. J. David Margerum, Dr. Shi-Yen Wong and Michael J. Little for liquid crystal material development. Peter W. Gregory and Anita L. Stoudt are thanked for their editorial assistance.

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SECTION I
INTRODUCTION AND SUMMARY

The Liquid Crystal Airborne Display program was a four-phase effort. Phase I began in April 1972 with an analysis of technology applicability; Phase II added work involving the evaluation of real display hardware; Phase III further extended the effort to the design and fabrication of a larger display; and Phase IV concluded the program with a study of assembly techniques for still larger displays. This report covers the work accomplished in Phases II, III, and IV; the accomplishments of Phase I have been previously reported[1].

The Liquid Crystal Airborne Display has been envisioned for many display applications, which may be categorized as:

- Directly viewed panel displays such as horizontal or vertical situation displays, status panels, or
- Indirectly viewed displays such as head-up displays, helmet-mounted displays, or displays with field-lens magnifiers.

During all phases of this program, reviews were held periodically to insure that the planned display technology would be suitable for the intended applications, completed in a reasonable time frame, and potentially cost effective.

Initially the Liquid Crystal Airborne Display was intended as a panel display for the presentation of synthetic array radar information, and thus the first phase, Phase I, began with a study of typical mission content, sensor performance, human operator requirements and the feasibility meeting these requirements with a liquid crystal display. Under Phase II, a one-inch square module containing 10,000 picture elements established the validity of the liquid crystal display technique for the presentation of real-time television or radar imagery. In this phase, display performance data was obtained for operator viewing ranging from nighttime to direct sunlight conditions. This data verified the validity of the original objectives

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[1] M. N. Ernstoff and R. N. Winner, "A Study of the Application of Reflective Displays to Synthetic Array Radar" Technical Report AFAL-TR-73-155 Air Force Avionics Laboratory, Air Force Systems Command, Wright-Patterson Air Force Base, Ohio.

established in Phase I for providing a cockpit panel display that could be superior to the CRT for all conditions of operational use. An important part of this effort was a series of experiments and performance measurements on operating devices as they lead to new installation arrangements for utilizing this new display component to maximum advantage. Essential to this phase was the careful photometric evaluation of semiconductor wafer topology and materials, a series of wafer smoothing experiments, and various electrode material compatibility tests on display brightness and contrast. From these and other test data, the ultimate performance of liquid crystal displays was determined for a variety of postulated applications.

During Phase II, the program was redirected to examine the capability of meeting the head-up display requirements with a Liquid Crystal Airborne Display. The advantages of a liquid crystal display for head-up display use were explained and demonstrated to the Department of Defense's Advisory Group on Electron Devices (AGED) using an operating breadboard mockup in December 1974 (see Figure 1).

Meanwhile attention was also being devoted to the economics of producing the display. There was concern that the yield of the required processing and fabrication procedures would never be sufficient to permit the displays to be fabricated on a production basis. A serious effort was mounted during the first half of Phase III (Phase IIIa) to eliminate the defects in the semiconductor chip used to form the basic matrix electrode structure for the liquid crystal airborne display. The project was relocated within Hughes by shifting the semiconductor processing from the state-of-the-art environment of the Semiconductor Research Laboratories in Newport Beach to the production environment of the Industrial Products Division in Carlsbad. Tight control of processing procedures was quickly obtained, and as a result, the first line-defect-free one-inch square display was built and demonstrated in June 1975. Although the goal had been only to eliminate line defects, element defects were essentially eliminated as well. The display exhibited only three defective picture elements out of a total of 10,000. Furthermore, it was established that the production of this line-defect free display was not an isolated case; several more line-defect free devices were obtained from subsequently processed batches of wavers and stockpiled for later use.

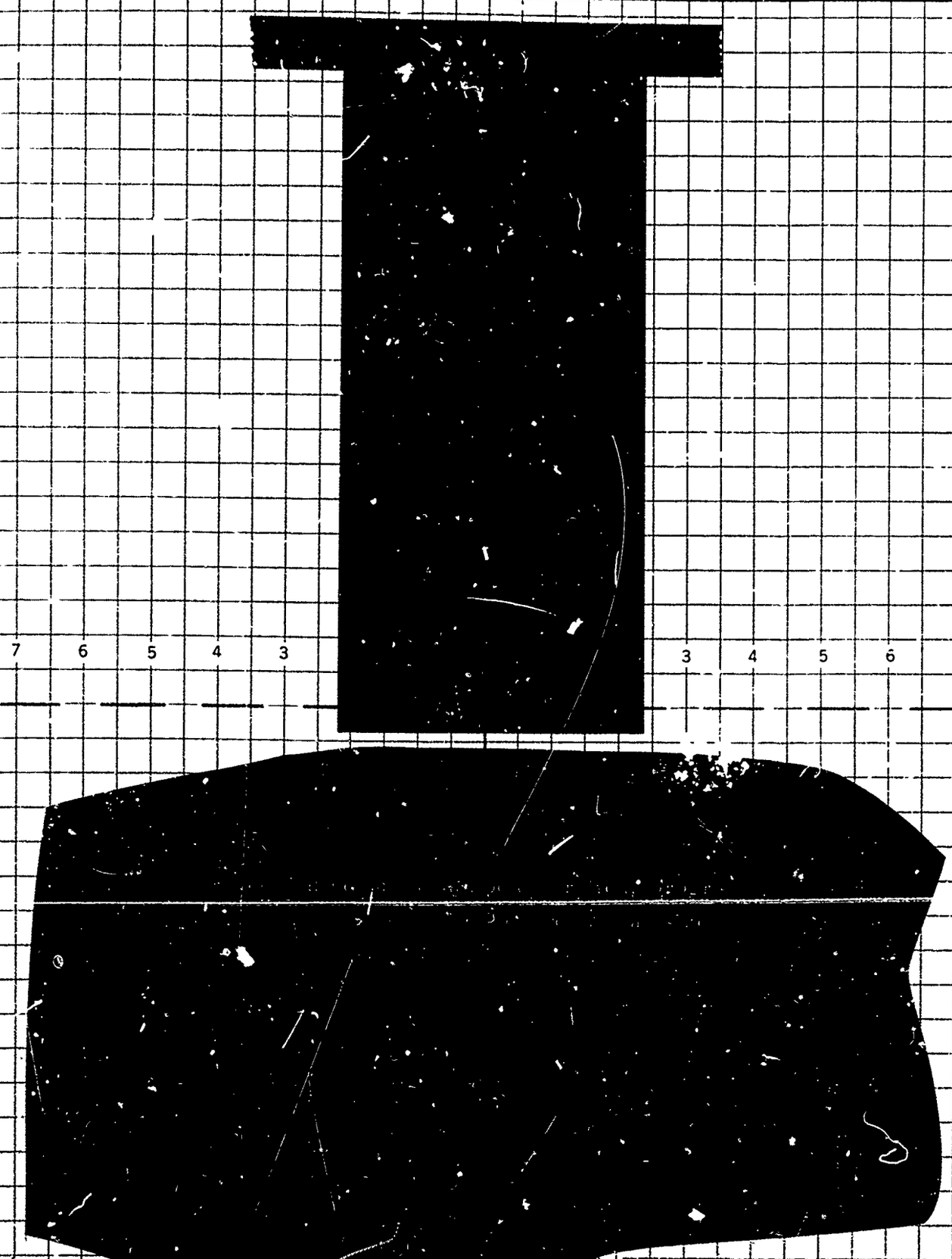
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Figure 1. HUD breadboard illustrating use of liquid crystal matrix for image generation.

Having proved that defects could be controlled, program emphasis was refocused on the steps necessary to meet the display size and resolution requirements. In Phase IIIb, four chips were arranged adjacent to one another in a square mosaic format (referred to as a quad), and a 2-inch square television display with 40,000 active picture elements was demonstrated in December 1975. Subsequently, in March 1976, work was begun on developing techniques for building up still larger displays by assembling mosaic arrays of modules. This work concluded with the fabrication of a conceptual model to show the feasibility of the wrap-around conductor interconnect technique.

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Each of the major events introduced in this brief chronological review are described in depth throughout the remainder of this report, beginning with Section 2. The balance of this section will summarize the program for those readers who wish a concise overview of the liquid crystal display technique, its application, and the future potential of the display method.

PROGRAM GOALS

The requirements for SAR display that were previously reported on[1] are briefly summarized below for convenience. The foundation for the recommended requirements appears in Appendix A.

Display Requirements-SAR Panel Display

- Display resolution . . . . . 1000 x 1000 pixels
- Display size . . . . . 10 x 10 inches
- Brightness/Reflectance . . . . 20 percent
- Video encoding . . . . . 4 bits
- Contrast Ratio 64:1
- Gray Shade Response ($\sqrt{2}$ luminance steps). . . . 13 shades under a 110 000 lux (10, 000 fc) ambient.

Requirements - HUD Display

Since the head-up display provides a virtual image of the display surface to the pilot, heavy importance is placed upon the optical specifications. Salient values, extracted from the military specification for Head-Up Displays (MIL-D-81641) are listed below.

- System error (maximum): 1 mrad central 12° FOV
  2 mrads $12\text{-}24^{\circ}$ FOV
  3 mrads 24° FOV
- Symbol linewidth: 1 ±0.2 mrad
- Reflection reducing coatings - all optics

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[1] M. N. Ernstoff and R. N. Winner, "A Study of the Application of Reflective Displays to Synthetic Array Radar" Technical Report AFAL-TR-73-155 Air Force Avionics Laboratory, Air Force Systems Command, Wright-Patterson Air Force Base, Ohio.

- Combining glass displacement error (maximum): 0.6 mrad central 12°
  1.2 mrads 12-24° FOV
  2.0 mrads 24° FOV

- Binocular disparity (maximum): horizontal divergence: 8.0 mrads
  horizontal convergence: 2.5 mrads
  vertical convergence: 1.0 mrad

Symbology requirements for the HUD are also specified in this document and they can be met by a liquid crystal matrix display source assuming a symbol generator capable of displaying this general class of information. The inherent stability of the matrix display provides a significant advantage over the CRT in the HUD application in that it can display symbology not only with the required precision of position, but with long term stability and at higher brightness.

Recommended values for the liquid crystal display symbology obtained from Appendix A are as follows:

- Character height: 30 min. of arc (8.7 mrads)
- Character width: 3.75 to 6 min. of arc (1 to 1.75 mrads)
- Dot matrix: 15 x 21 pixels
- Pixel (dot) spacing: 1.4 min. of arc (0.4 mrad)
- Pixel size: Approx 0.4 mrad square

The requirements consider the use of dot matrix characters and symbols rather than other types, since the liquid crystal matrix display has been developed for television display and does not provide for stroke-writing or modes of operation other than raster scan.

To meet the HUD requirements for current inventory aircraft such as F-16, the following would also apply.

- Lens aperture: 5 inches
- Field of view: 11° Vertical x 16° Horizontal instantaneous (26 inches viewing distance)
- Allowable head movement: 2 inches vertical x 3 inches horizontal

• Display size	6.8 inches wide x 6.6 inches high x 21.5 inches long plus combiner
• Symbol brightness	5500 cd/m^2 (1600 fL)
• Symbol contrast	1.2
• Combiner reflectivity	20 percent
• Combiner transmission	75 percent
• Symbol line width	1 ±0.3 mrad

Liquid Crystal Display Goals

Based upon the foregoing requirements, data gathered from performance measures conducted on 1 x 1 inch display modules, and various test cells, the following performance goals were established for the Phase II and Phase III development effort.

• Resolution	100 pixels per in.
• Sizes	1 x 1 in., and 2 x 2 in.
• Contrast Ratio (maximum)	24:1 at optimum viewing geometry
• Contrast Ratio (minimum)	Not less than 12:1 within a solid angle ±15 deg. from normal to azimuth and ±5 deg. in elevation
• Reflectivity	80% of an ideal lambertian surface
• Writing Speed	Compatible with Standard TV 60 field/sec, 2:1 interlace
• Response time	Equivalent to P 4 phosphor, or 33 msec. decay to 10% point
• Dynamic Range	8 shades-of-gray under all values of ambient illumination to a maximum of 110,000 lux (10,000 fc)
• Quad (2 x 2 in.) Assembly tolerance	Gaps between adjacent wafers not to exceed 0.0016 in.
• Defects	Less than 40 randomly distributed visible elements per individual 1 x 1 in. module. No entire row or column defects. Quads shall be assembled from 1 x 1 modules meeting these criteria.

The goals for phase IV were to:

1. Identify a technique suitable for display modules interconnection for the fabrication of larger displays by assembling mosaic arrays of modules;
2. Fabricate a conceptual module to show how the selected technique would be implemented in a physically and electrically analogous manner to that required for a real display.

WHY LIQUID CRYSTAL DISPLAY?

Cockpit panel displays are relatively easy to implement under subdued or nighttime lighting conditions. Under direct sunlight, the problem of displaying high resolution shades-of-gray information on any kind of light-emitting display has been difficult and sometimes impossible to achieve. Filtered CRT's and incandescent alphanumeric readouts are the two most prevalent categories of light-emitting cockpit displays that can be seen in daylight, however, their typical performance is usually far from the desired ideal.

A relatively new class of component, light-emitting diodes (LEDs), has also been used where a limited number of elements are required in the matrix. Unfortunately, the conversion efficiency of existing LED's is low and to achieve even a modest number of dot elements for an alphanumeric display it requires significant input power. As an example, a display consisting of 14 lines with 22 characters per line would require 50 amps. In the calculation of this example it is assumed that 15 of the 22 characters are emitting. Each character is comprised of 16 segments, and an average of eight segments per character will be activated. Output brightness would range from 2700 to 6200 cd/m^2 (800 to 1800 fL) depending upon the diode type selected. The average current per segment at this brightness would be 30 ma for a 1/2 amp 100 μsec-wide drive pulse with a 1.5 msec duty interval. Thus, alphanumeric and symbol content must be kept simple (few dots and few characters) to best use the LED device.

Other more efficient matrix display techniques, such as plasma display and electroluminescence have not achieved the desired output brightness for daytime display use. Electrochromic techniques are being watched with interest because of their high reflectivity and very wide viewing angle, but their performance has not yet achieved the repeatability, longevity, or immunity from vibration that is required for airborne use.

Advantages/Disadvantages of Prior Art

The cathode-ray tube (CRT) has historically been used for sensor and weapons system display functions, but it has always been contrast limited when subjected to the high ambient illumination conditions encountered in daytime flight. With direct sunlight illumination, the contrast ratio (on-brightness/off-brightness) of a CRT display is typically limited to a very low value in the range of 2:1 to 3:1; the exact value depending upon the indicator faceplate treatment. Using a standard "rule of thumb" for predicting the maximum number of gray shades perceived by a human operator using a continuous tone display with a given contrast ratio (see equation), the CRT display is limited under high ambient lighting conditions to three to four shades of gray at best,

$$\text{Contrast Ratio} = \sqrt{2}^{N-1}, \text{ where N = number of } \sqrt{2} \text{ gray shade steps.}$$

The system disadvantages of the CRT are its poor visibility under direct sunlight, its length (in high-resolution configurations), its need for a high-voltage power supply, and its deflection system which is an open-loop analog method subject to error and drift. The chief advantage of the CRT is that it is highly evolved component that has been in production in various forms for nearly half a century, hence its price is low, and its behavior is well known. Although improvements are still being made to the CRT's, there is no reason to expect the order-of-magnitude quantity of contrast improvement that is desired for daylight operation.

Performance of the Liquid Crystal Matrix Display

The reflective liquid crystal display approach of this program has demonstrated its potential for replacing the CRT in future military applications where good visibility is required under high ambient illumination. The liquid crystal display makes use of ambient illumination to create an image rather than emitting any light of its own, hence its contrast ratio remains constant as the level of illumination increases. The liquid crystal pictorial display is thus an improvement rather than merely a replacement for the CRT's that have been historically used for this function, and this fact is confirmed by measurements conducted on working display modules and test cells.

In Figure 2, the contrast of an operational liquid crystal display is compared with that of a state-of-the-art high performance CRT and filter

combination, and with that of a liquid crystal test cell having a smooth surface and a high reflectivity electrode. The latter, although not capable of displaying television, represents a level of performance that could be realistically attained from the present display with application of known surface improvement techniques. The data for the existing matrix display indicates that its contrast is already superior to that of the CRT under very high ambient lighting conditions. The contrast ratio of the present liquid crystal display is typically 15:1, and the projected performance based upon test cell data is over twice that. The high visibility of the liquid crystal display has been demonstrated under severe ambient illumination as the photograph in Figure 3, taken under 110,000 lux (10,000 fc) of sunlight illumination, shows. Thus, the Liquid Crystal Pictorial Display is the first technology to permit real-time gray-scale television imagery to be presented under viewing conditions comparable to, and as severe as daylight tactical aircraft operation.

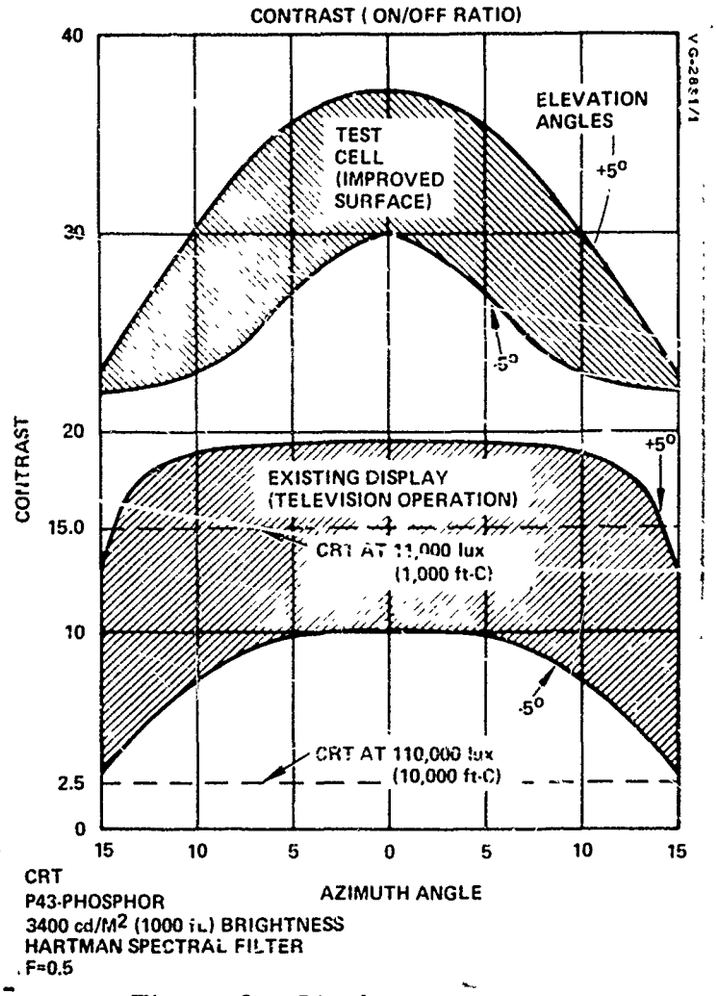


Figure 2. Display contrast.

LIQUID CRYSTAL MATRIX DISPLAY OPERATION

Electro-Optical Characteristics

A simplified cross section of an elemental display cell is shown in Figure 4; it consists of a thin film of dynamic-scattering liquid crystal material sandwiched between a reflective, mirror-like electrode and a transparent conductive electrode. A voltage difference between the electrodes induces a current flow through the material which, in turn, causes

Figure 3. Visibility in direct sunlight.

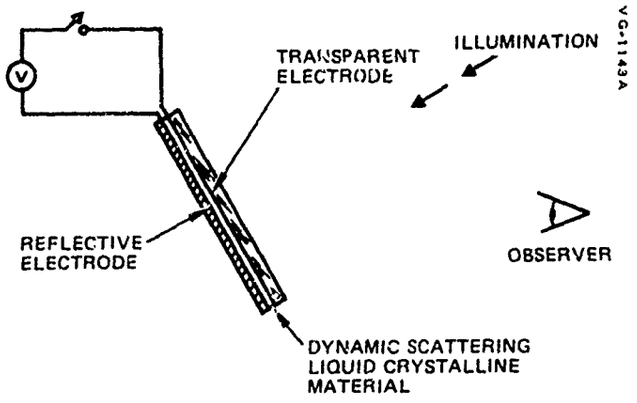


Figure 4. Reflective liquid crystal cell.

hydrodynamic turbulence in the material. The resulting dynamic scattering[2] is approximately proportional to the amplitude of the applied potential.

In the OFF state, with no electric potential applied to the electrode, the liquid crystal material is clear and the viewer sees whatever is specularly reflected by the display (see Figure 5a). When the display is positioned correctly with respect to a dark 'light trap,' the reflection of

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[2] G. H. Heilmeier, L. A. Zanoni, and L. A. Barton, "Dynamic Scattering: A New Electro-optic Effect in Certain Classes of Nematic Liquid Crystals," Proc. IEEE, 56, 1162, July 1968.

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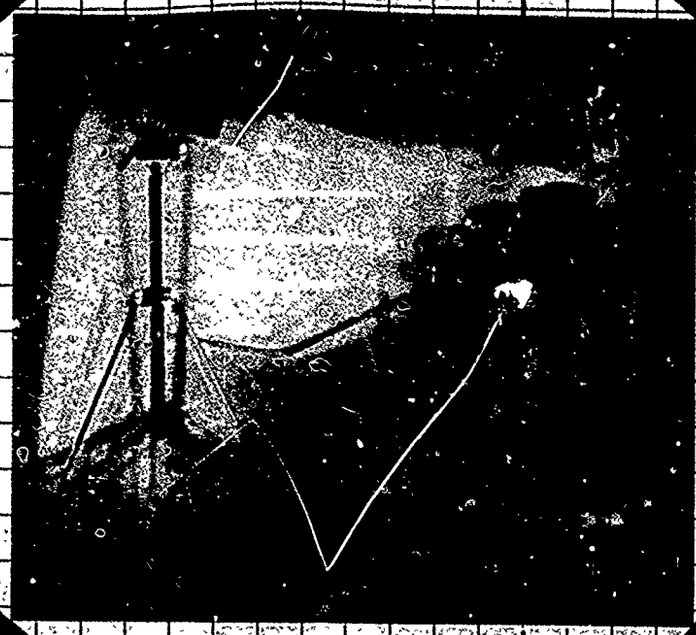


Fig 3 DX

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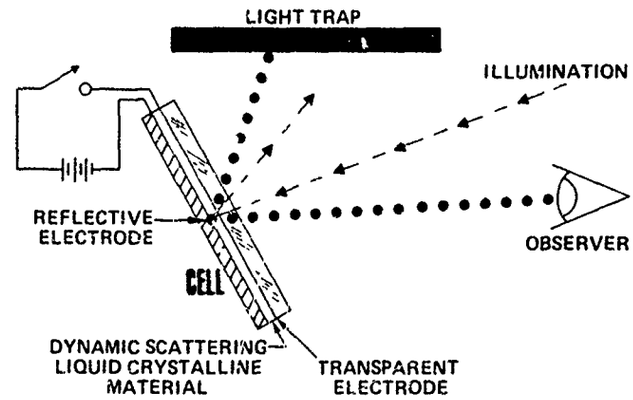
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Fig. 10 DX

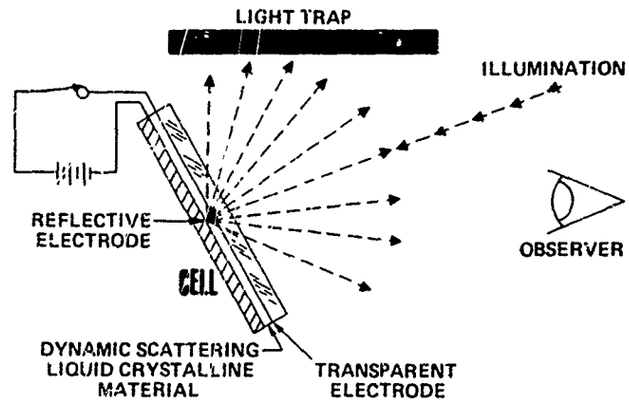
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its dark surface in the electrode makes the elemental cell appear black.

In the ON state (Figure 5b) an electric potential is applied, and the resulting dynamic scattering causes the display to appear a frosty white, as some of the incident illumination is reflected to the observer. Note that the illumination and the observer are both on the same side of the display. Shades of gray can be obtained because the magnitude of this diffuse reflection is proportional to scattering level and, hence, to the applied potential.



a. OFF CONDITION



b. ON CONDITION

Figure 5. Liquid crystal cell operation.

Display Construction

The basic display module is fabricated by placing liquid crystal material between a transparent conductive electrode and a one-by-one inch simiconductor chip as shown in Figure 6. A two-by-two inch quad, or larger display is achieved by assembling mosaic arrays of chips as shown in Figure 7, a and b. The transparent conductive electrode for either display is a thin continuous film applied to the cover glass. The matrix array of elemental reflective electrodes that spatially define the individual picture elements is on the surface of the semiconductor chip. Each reflective electrode serves as an electrical contact to the liquid crystal material and as an optical reflector. The film of liquid crystal material that fills the cavity between the transparent electrode and the semiconductor chip is common to the entire array of elemental reflective electrodes.

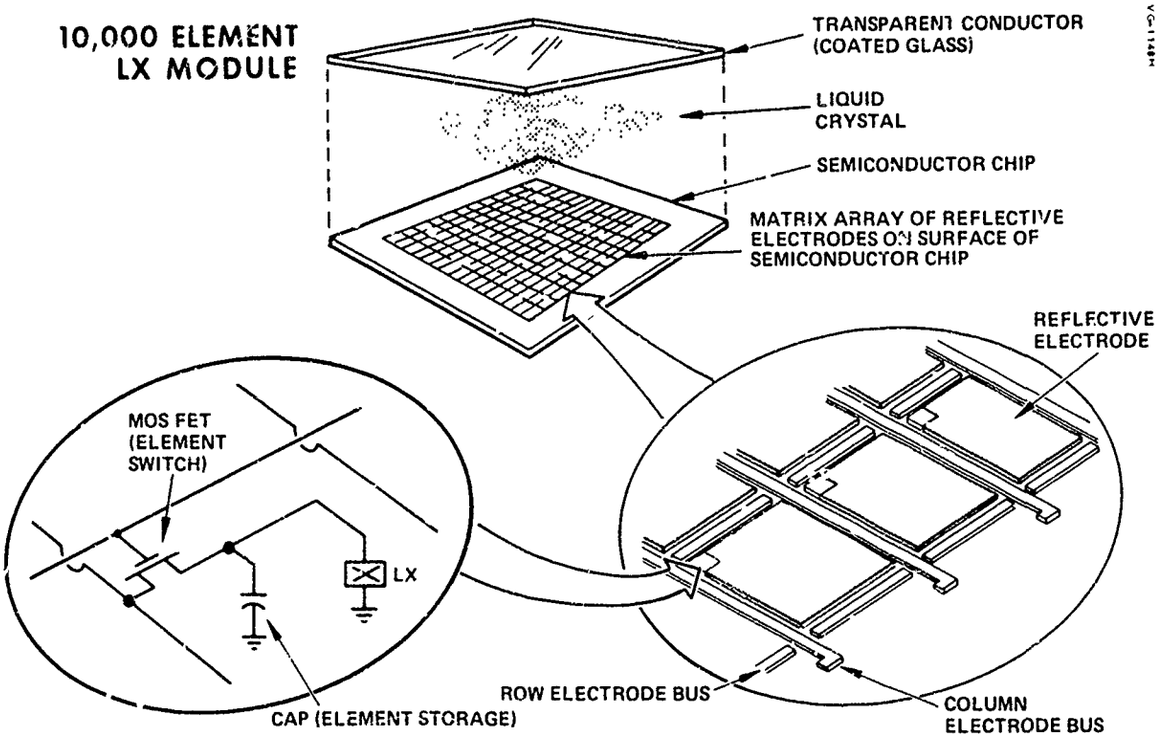
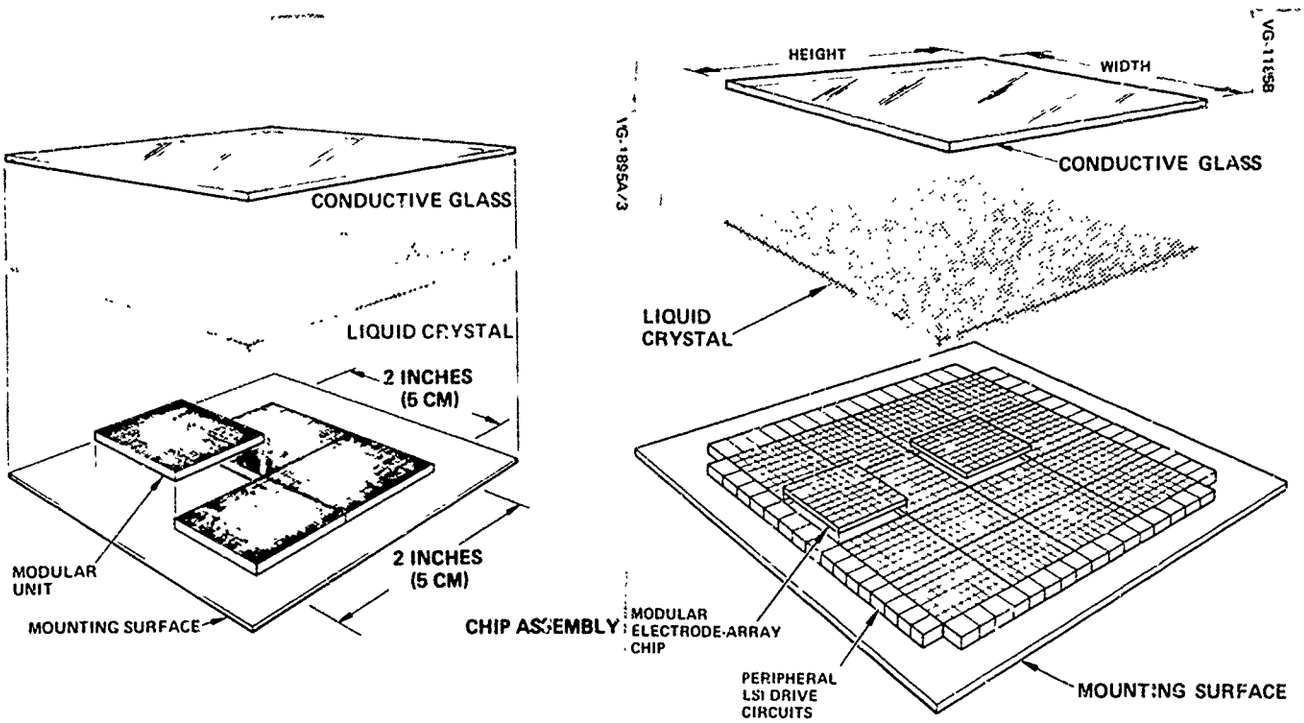


Figure 6. Basic display cell.

This thin film of material need not be partitioned, because the ratio of its thickness to the size of the elemental reflective electrode is small enough to effectively prevent any crosstalk between elements. (See Figure 8.) The interstitial spaces between the electrodes have also been kept small so that the active area of the display is more than ninety percent of the available source area.

The matrix array of elemental electrodes, as well as the underlying circuits that control the electric potential of each individual element, are formed economically in and on the surface of a bulk silicon substrate by using large-scale-integration (LSI) semiconductor circuit technology (see Figure 6). With LSI fabrication techniques, all of the elements in the matrix array are formed concurrently. The processing operations for making the disc-shaped wafer, from which the square chip is later cut, involve the use of a set of masks, each engraved with a variation of the repetitive pattern of the matrix structure. By an appropriate processing sequence employing



a. Liquid crystal quad display. b. Liquid crystal mosaic array display.

Figure 7. Large area liquid crystal arrays.

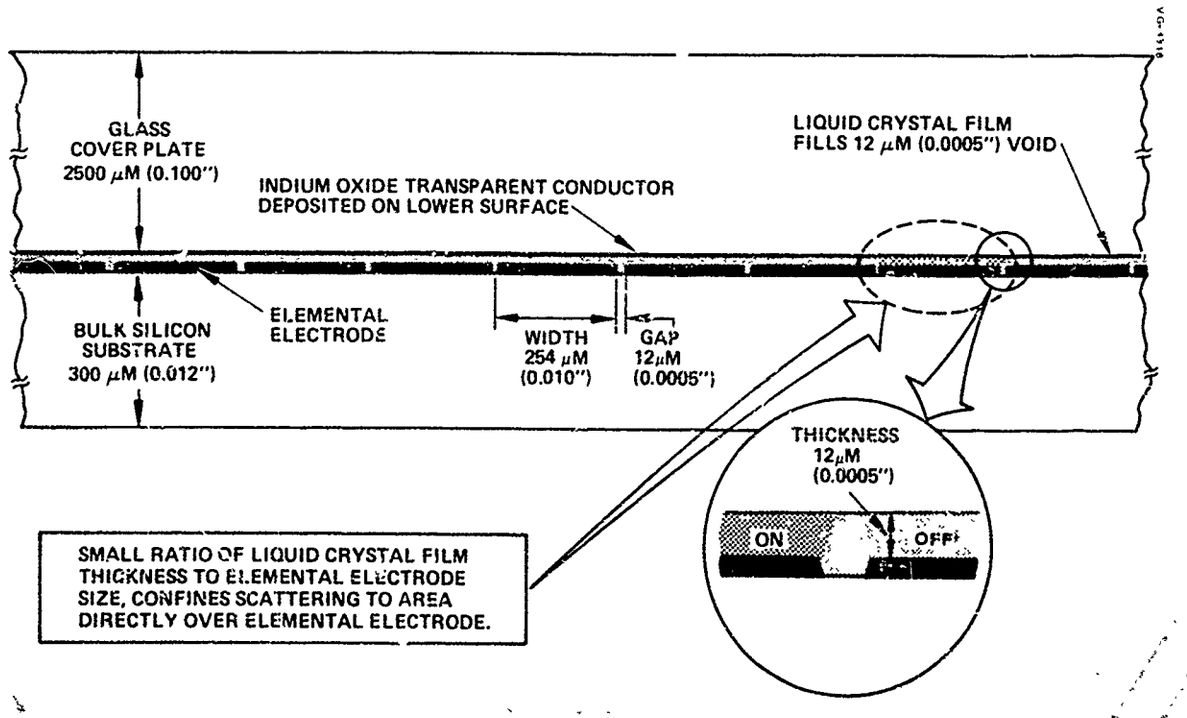


Figure 8. Cross section of assembled cell.

photolithographic etching, material deposition, and semiconductor-doping steps, the required circuits and electrode structure are formed (see Appendix B). Metal-oxide semiconductor (MOS) circuit fabrication on bulk silicon was selected over other technologies such as silicon-on-sapphire (SOS), or thin-film transistors (TFTs), because it is a mature, rather than a developing, technology.

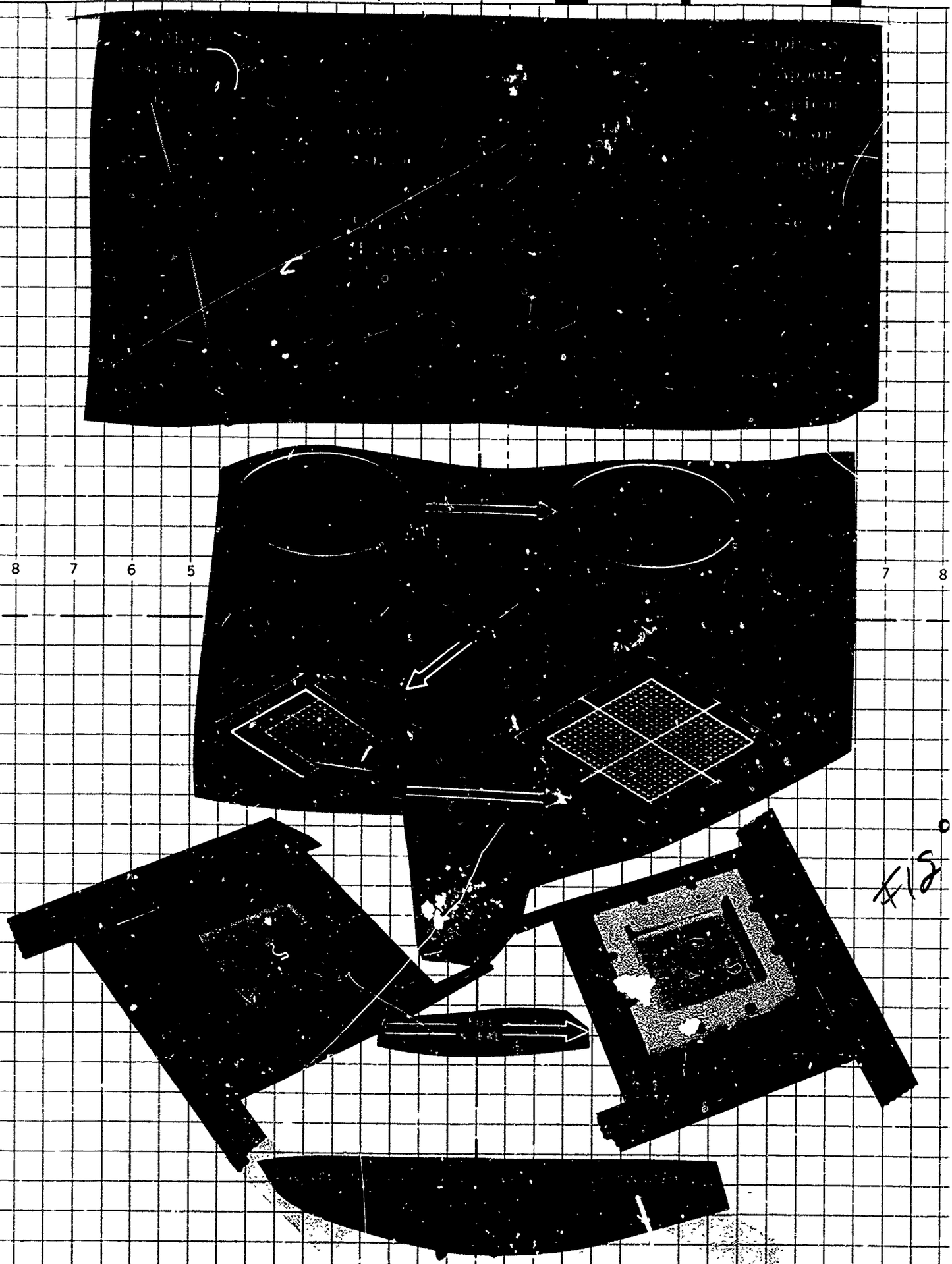
Figure 9 shows the steps in the fabrication of a quad array, as assembled from the same kind of 1 x 1 inch chips that are used in the construction of the single-module display.

Placing an image on the display requires two distinct operations: (1) converting the incoming video data into a matrix display format, and (2) channeling that data to the appropriate elements in the matrix array. The circuits responsible for reformating the incoming data are referred to as drive

Figure 9. Quad module display fabrication.

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circuits, and those for channeling the signals to the individual elements are called the addressing circuits.

The liquid crystal display (module) contains the necessary addressing circuits within its substrate to achieve television operation. Both the drive and addressing functions are basic to the operation of the single module, the 2 x 2 quad, and all larger displays and they will now be described.

Drive and Signal Interface

The drive circuits have presently been implemented separately from the display using conventional components. Ultimately the drive circuits will be microminiaturized using LSI techniques and could be positioned around the periphery of the display as shown in Figure 10. The addressing circuits are an integral part of the display chip, and are intrinsic to the electrode-array of picture elements. By using separate chips to perform the drive and addressing functions, significantly higher device yields can be achieved; not only is each clip simpler, but the components can be pretested before assembly.

A block diagram of the display and its drive circuits is shown in Figure 11 for the situation in which the data source is a single video channel. The Liquid Crystal Pictorial Display is addressed a line-at-a-time rather than an element-at-a-time as is the usual practice with CRT television displays. Line-at-a-time addressing was selected because it permits the use of the simplest acceptable addressing circuit, a single transistor and capacitor. With line-at-a-time addressing, all the elements in any given line are written simultaneously. Each line of the display is written sequentially from top to bottom until an entire image has been generated. The

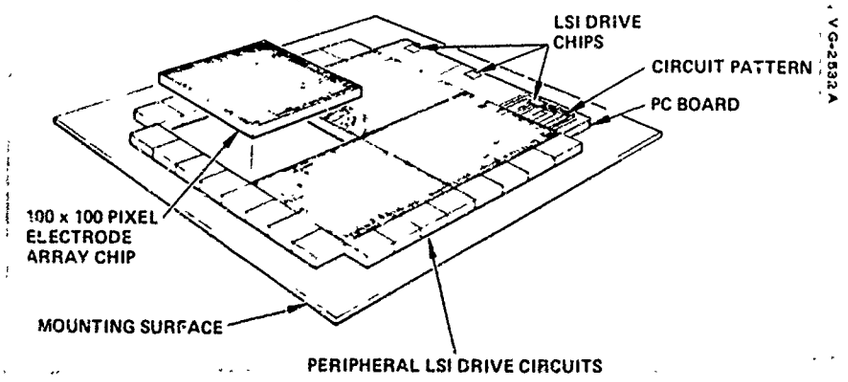


Figure 10. Peripheral placement of LSI drive circuits.

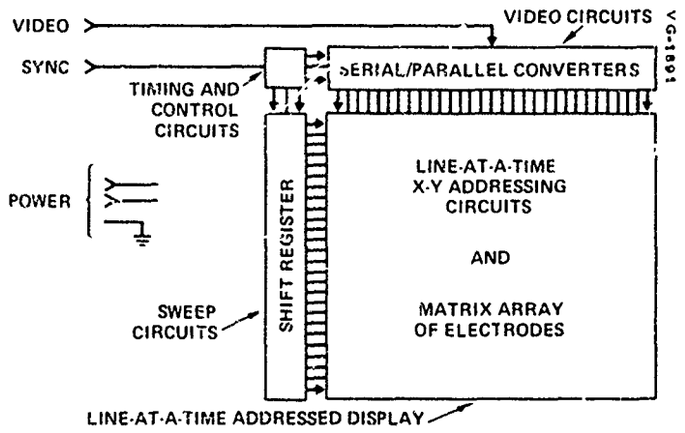


Figure 11. Functional blocks and electrical interface.

complete image generating sequence is repeated 30 times per second to provide a flicker-free presentation of moving images.

Line-at-a-time addressing requires that all columns of the display be driven in parallel with separate and distinct video signals. When the video data source is a conventional standard TV signal whose data are in a serial format, the necessary video signals can be derived from the input signal by performing a serial-to-parallel conversion. The serial-to-parallel conversion of analog video is analogous to the serial-to-parallel conversion of digital data, but different in that the magnitude of the signal must also be preserved. Dual serial-to-parallel video converters, alternating their functions, can collect the serial data while simultaneously outputting previously collected data to a line in parallel form. The sweep function is performed digitally by a simple shift register propagating an 'enable' pulse to determine which line is written. The updating of the video data is stepped in synchronism with the shift register. When the drive circuits are integrated with the display using hybrid packaging techniques, the result is a display system with a simple and conventional electrical interface, i. e., analog video, sync, and power.

A circuit diagram of the addressing circuits contained within the basic electrode-array chip is shown in Figure 12. Associated with each elemental cell or picture element is a transistor-capacitor sample-and-hold circuit and a reflective electrode. The function of the sample-and-hold circuit is to

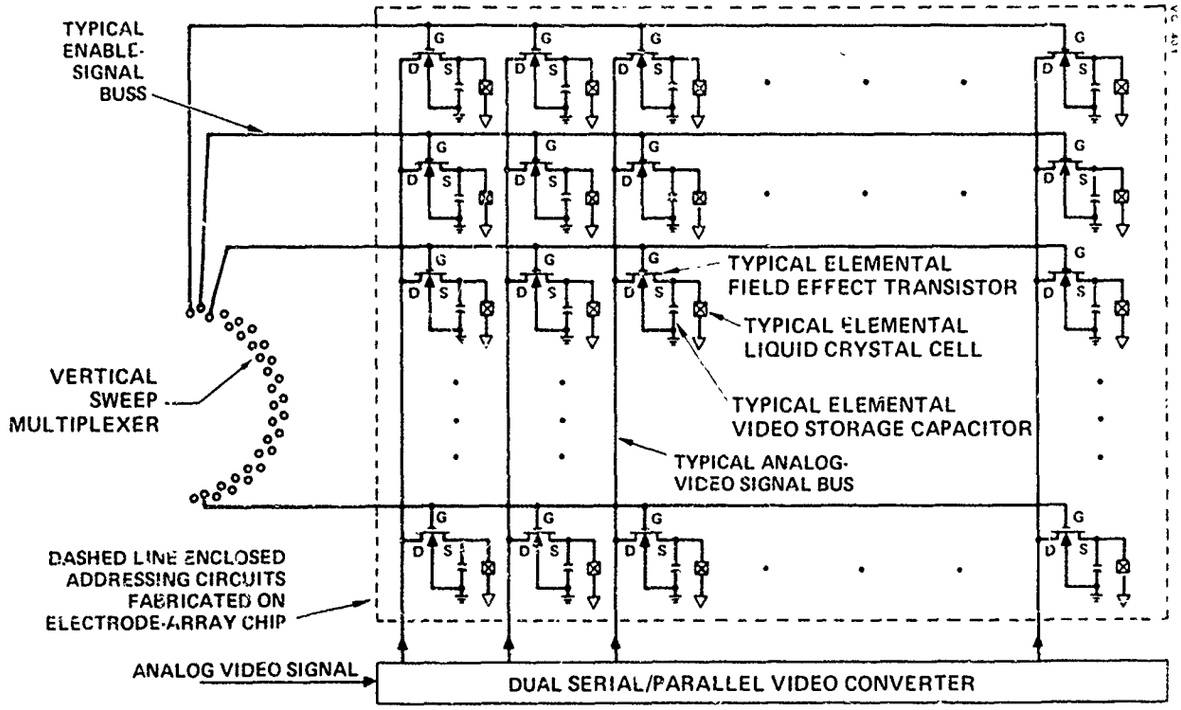


Figure 12. Addressing circuits.

stretch the incoming analog video signal pulses, delivered during the microsecond long addressing pulse interval to the millisecond length analog signals required to excite the liquid crystal material. This pulse stretching circuit makes it possible to build a real-time display using liquid crystal materials that are comparatively slow with respect to the elemental addressing rates.

Further examination of the electrical circuit of the Liquid Crystal Pictorial Display will show that as a matrix display it can have a unique advantage in very high resolution display applications. In the case of a 1024 x 1024 picture element resolution display being refreshed at a 30-Hz rate, a 16-MHz bandwidth video channel is required for the data in a conventional single channel system. A Liquid Crystal Pictorial Display permits the use of multiple, low-bandwidth, video channels. One is thus given the alternative of providing sixteen 1-MHz video channels, which may be implemented with integrated operational amplifiers, as opposed to providing a single channel 16-MHz discrete component video amplifier. If the data to be presented are digitally scan converted imagery, this option may also simplify the organization of the scan converter memory system.

KEY ACCOMPLISHMENTS

The work accomplished on this program has proven the liquid crystal display to be potentially suitable for a wide variety of applications; for direct-viewing through a modular approach to large panel mosaic arrays, and for magnified viewing (HUD, HMD, and etc.) through increased resolution density on the unitary module used for the final assembly. Feasibility of the technology has been investigated through working models and in some cases through simulated hardware to verify processing techniques. The content of the work ahead lies chiefly in applications engineering and in manufacturing methods technology.

Defect-Free Display

Of the hundreds of wafers processed experimentally, most were sacrificed in experiments for improving process development, calibration, and device evaluation techniques; a natural tendency in an advanced development program. Eventually, enough standardization was achieved in the R&D program to permit the complete fabrication of over 20, 1 x 1 in., 100 x 100 pixel display modules and four quad arrays (200 x 200 pixel) modules. A photographic review of typical 1 x 1 displays produced during the development effort appears in Figure 13 and a photograph of the first quad array to achieve partial operation appears in Figure 14. What is presented in these two figures occurred under a research laboratory environment rather than the more closely regulated conditions found in production and is now largely historical. In 1975, Hughes took the first step toward standardizing the fabrication processes by transferring the liquid crystal project to its Carlsbad, California MOS production facility. This resulted in a reduction of display defects and the elimination of line defects. Also, having previously identified the mask defects and process-vulnerable steps contributing to defects, the feasibility of achieving high yield was improved as well.

Illumination and Viewing

The liquid crystal display component is essentially a flat panel display, although somewhat less flat than the ideal due to the practical need for light trapping and auxiliary illumination. (Refer to Figures 5a and 5b, page 11, and the accompanying discussion on electro-optical characteristics that begins on page 9.)

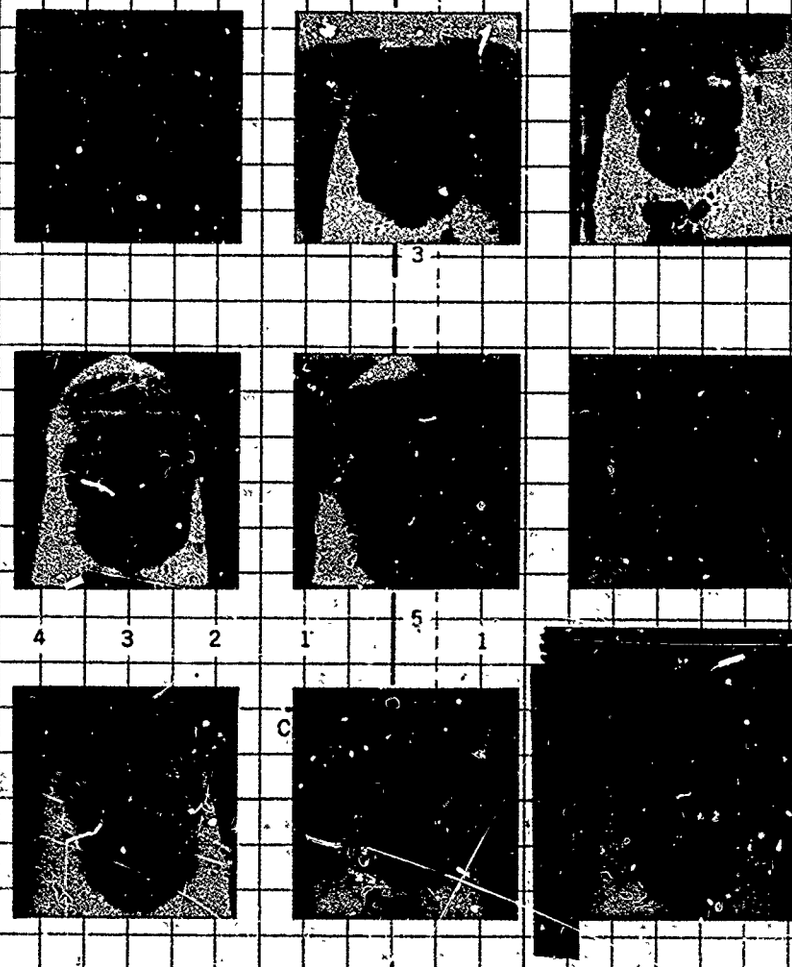
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Figure 13. Liquid crystal module - development history leading to defect-free display.

Figure 15 illustrates several operating mockups where light trapping is used. In Figure 15a, a simple curved light trap overhanging the T-33 instrument panel was sufficient for a small gray-scale display shown directly at the top center of the instrument panel. In Figure 15b, a simulated flat panel

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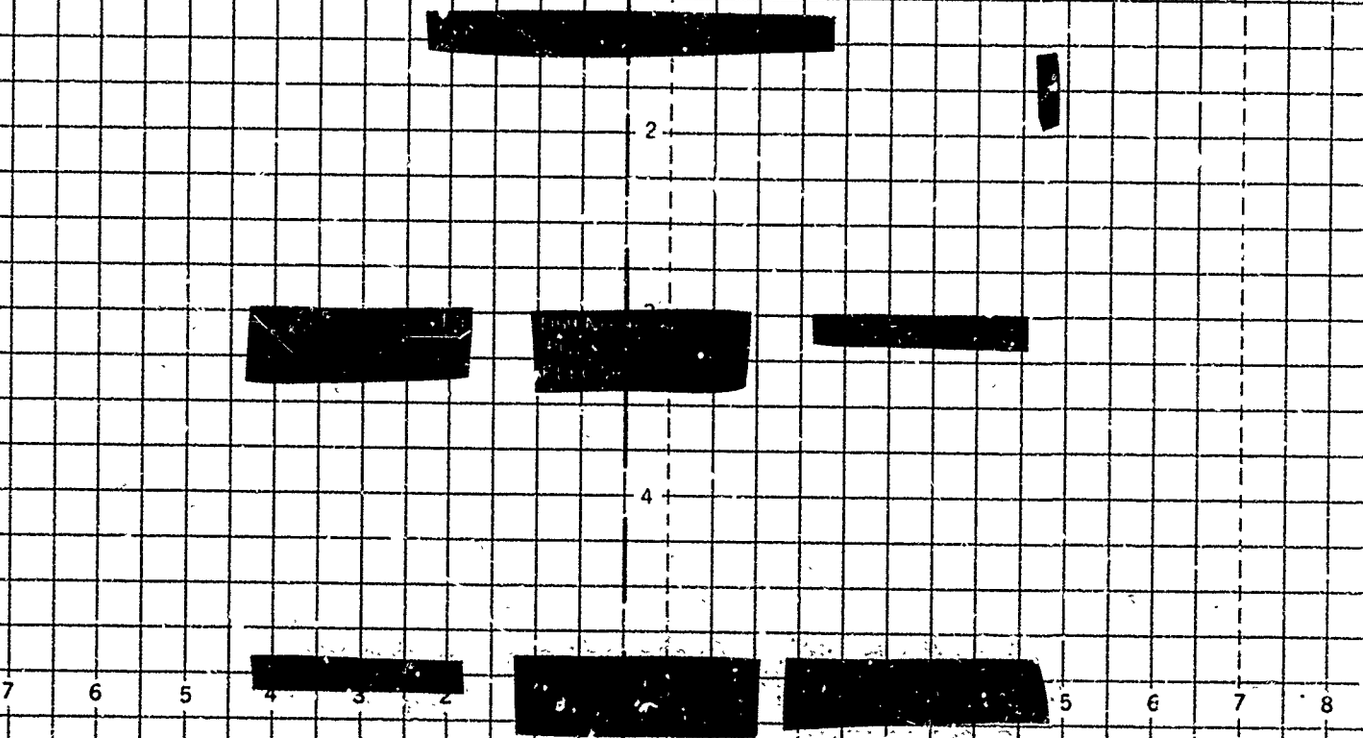


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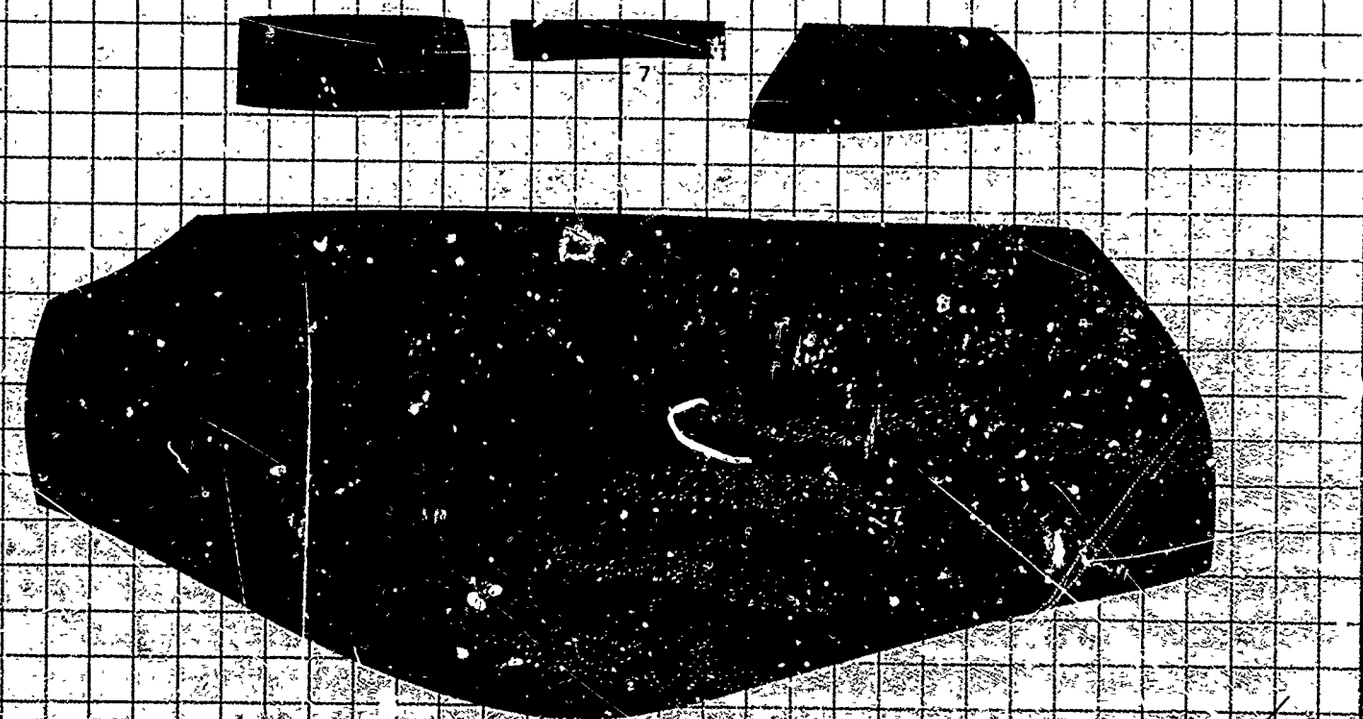
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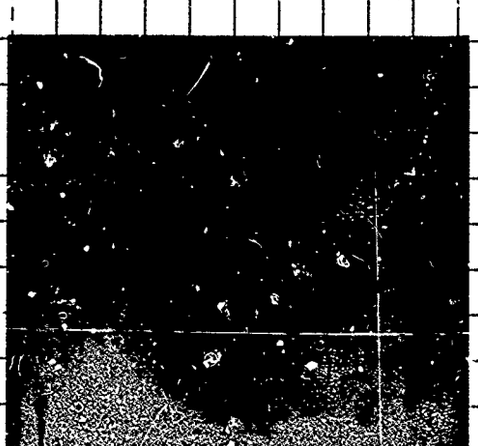
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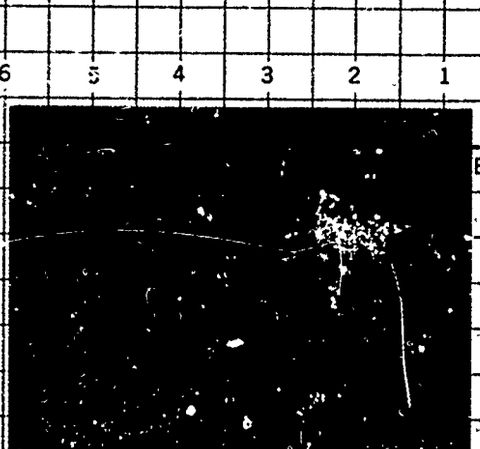
Figure 14. Development history leading to higher resolution, 40,000 picture element quad display.

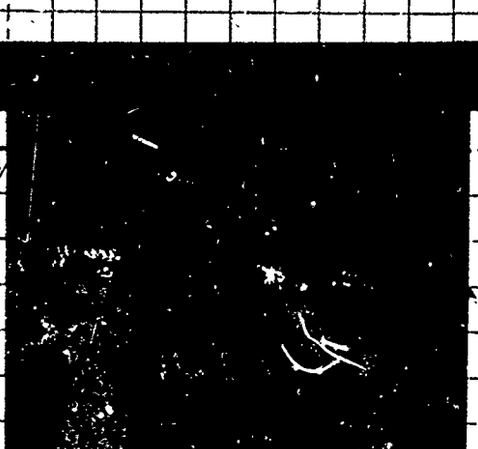
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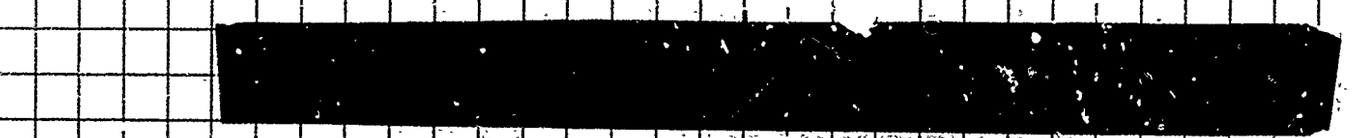
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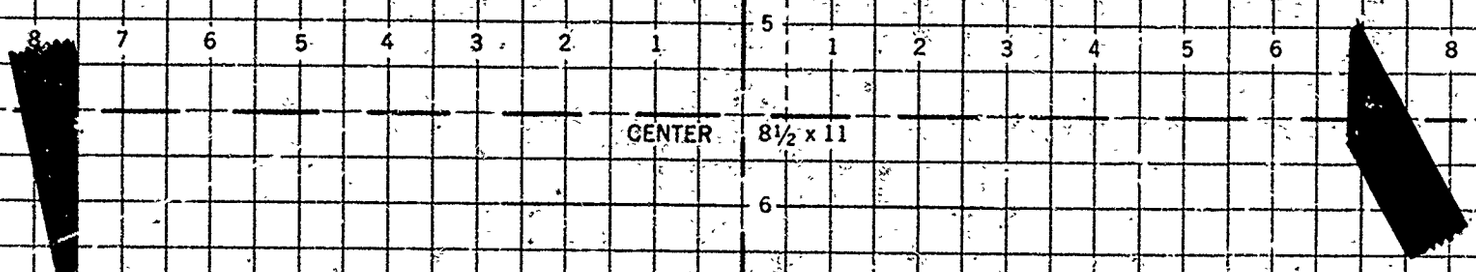
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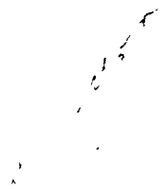








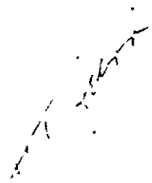
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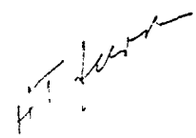
a. T-33 in sunlight.



b. Liquid crystal display and light trap added to front of F-4 HUD.



c. Another means of adding liquid crystal display to F-4 HUD.

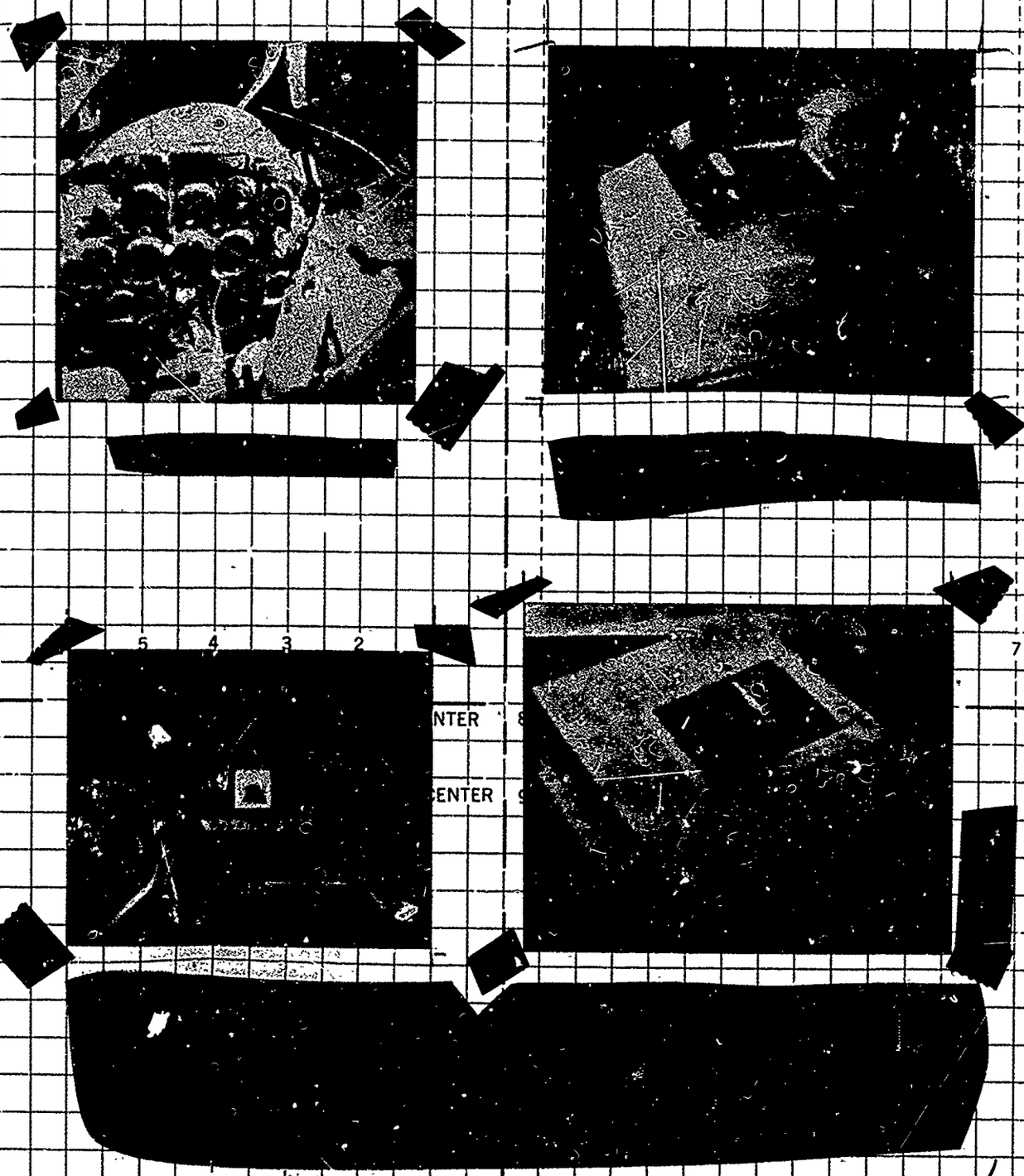


d. Wedge lighting for night viewing.

Figure 15. Installation and viewing for liquid crystal display.

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display using a large advertising alphanumeric (TCI) has been added to the front of the optical box used in the F-4 aircraft for HUD and optical sight components. Previously, this prime viewing space was only useful in the F-4 knobs and switches, because the space behind the panel could not be interfered with by display components such as CRTs that would intrude into the optical path. The overhead light trap contains a miniature fluorescent lamp within its front edge and is slotted at the rear edge; thus admitting direct sunlight where needed, while blocking sunlight from entering the display from any angle that would result in specular reflections directly back to the pilot. In Figure 15c a recessed arrangement is used which provides the function of light trapping and houses auxiliary lamps used for edge-lighting the display. This arrangement has the disadvantage of requireing additional panel depth, approximately 3 inches, and more seriously causes obscuration of the active display area for extreme off-axis viewing as would occur in side-by-side installations. It is good for single place installations, if the requisite panel depth is available. In Figure 15d a wedge lighted arrangement for night viewing is shown. The arrangements shown in Figure 15 are useful for illustrating the excellent visibility that can be obtained from the liquid crystal display under actual viewing conditions, including direct sunlight. In fact, the display in Figure 15b has been demonstrated half in shadow and half in 1000, 000 lux (10, 000 fc) incident sunlight with no loss in visibility.

The units illustrated in Figure 14 are also representative in thickness ($\approx$ 0.4 in.) for displays of their size. Larger mosaic arrays will require more LSI drive chips. Locating these entirely around the periphery may not be possible and connecting to a rear circuit board arrangement may be necessary to contain these functions. If this method is required, total panel thickness is still likely to be well below 2 in. (5 cm) for the basic display, not counting light traps, auxiliary illumination, or interface electronics.

Quad Display

The manufacturing techniques and masks developed for the single 1 x 1 in. module were used to stockpile a quantity of wafers for subsequent quad assembly. The wafers were sorted into two categories: (1) those with low defects, and (2) those with no line defects and very few element defects.

The semiconductor chips were selected to meet these criteria using an in-process test involving a probe station for electrical checks and a direct-visual test of performance by activating the semiconductor wafer on a television signal in a demountable test station apparatus. This was done with liquid crystal material prior to wafer cutting. The latter permitted photographic records of performance to be taken both before cutting and after final assembly operations. Four quad displays were constructed and they appear in Figure 14. The fabrication of the first three displays was primarily intended to provide information and experience in the various manufacturing operations. The fourth display was the product of this experience and served as a model for evaluation of the performance that can be expected from the modular construction techniques developed thus far.

The performance of the quad display was measured in terms of normal display parameters such as brightness, contrast, surface defects, and uniformity. Details concerning its operation are discussed in Section 6 of this report.

An important step toward making television display on the quad possible was the development of a very high density connector with 100 conductors per linear inch (≈39 conductors per cm). (See Figure 16.) This connector has provided a reliable and compact means for connecting to the display surface. The success of this connection scheme provides an alternative to placing the drive circuits adjacent to the display surface. The approach to be taken for fabricating the drive circuits is dependent upon the desired balance between development cost and manufacturing cost. All of the displays built to date have used discrete component drive circuits. This has minimized development cost, by permitting the display and the drive circuits to be optimized independently.

Interconnect Conceptual Model

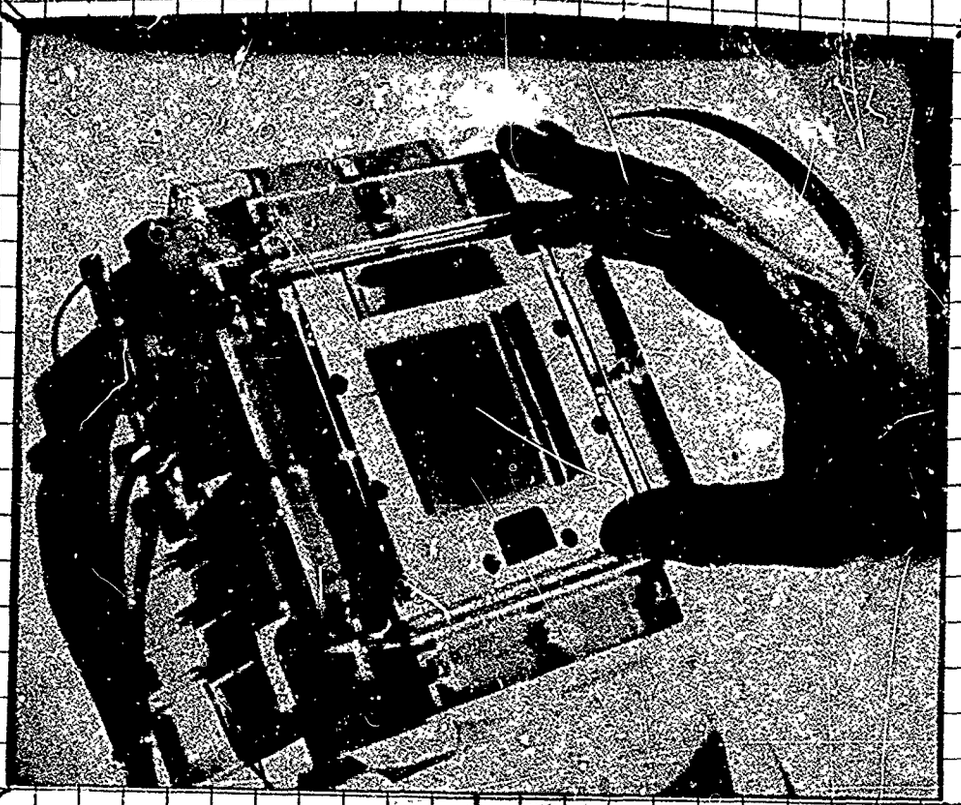
Several techniques were investigated for interconnecting modules into large area mosaic arrays. These multi-module techniques can be classed into two basic approaches: interconnection schemes which bridge modules together to form a large display surface; and self-contained schemes which place many autonomous display modules in proximity. Some of the techniques studied were applicable to only one of these approaches; others were applicable to both.

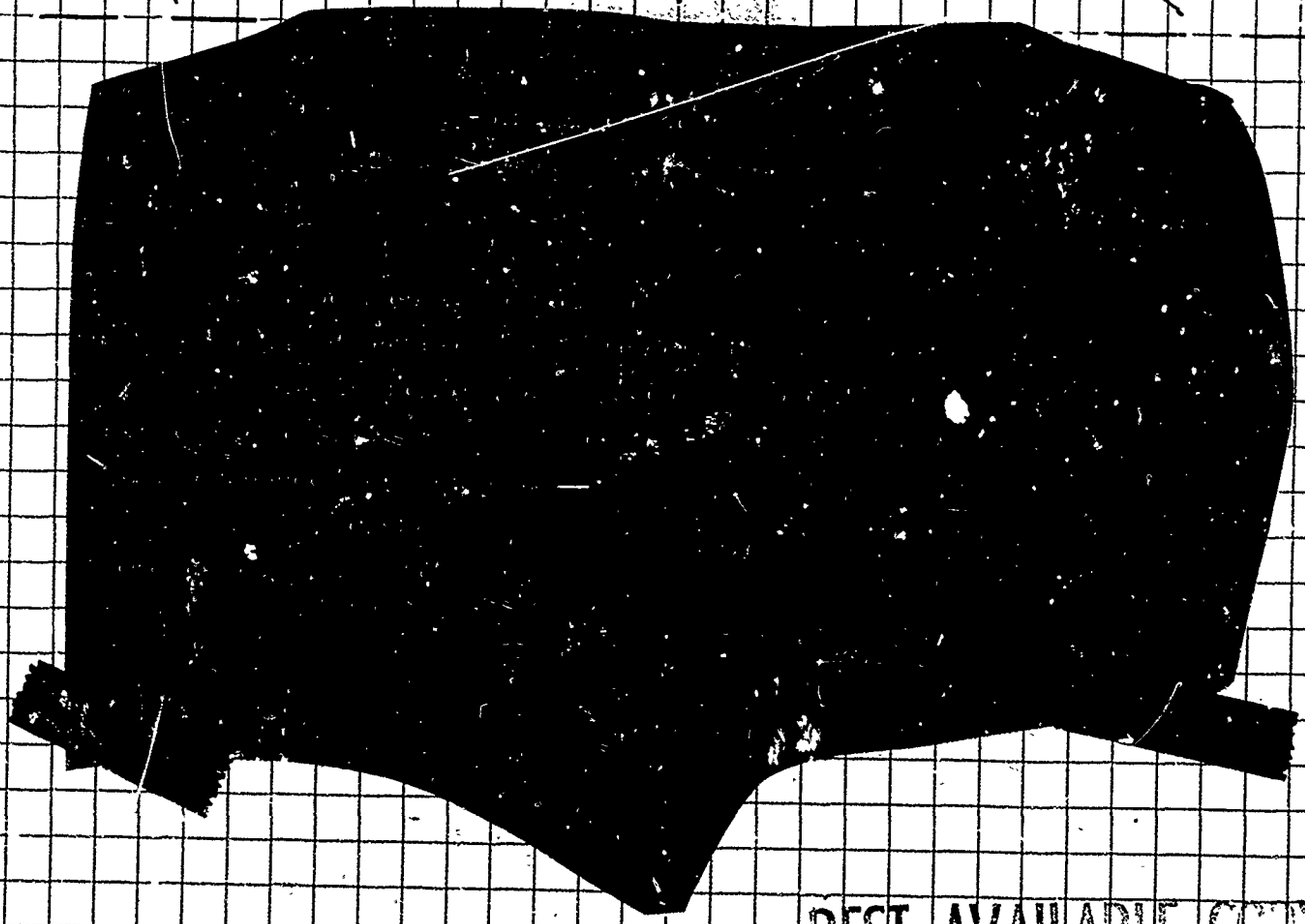
Figure 16. Display with high density connector.

A preliminary trade-off limited the choices available to two techniques: (1) bridging; and (2) wrap-around conductors with rear contacts. The former was considered the most straight forward to implement at the present time, but is limited to use with the interconnected module approach. The latter technique can be used with either the interconnected or self-contained module approaches, and because of this greater flexibility, it was selected for implementation in the form of a conceptual model. The conceptual model showed the feasibility of using the wrap-around with rear bump technique for interconnecting two modules at a density of 100 conductors per linear inch, and it successfully established a technology base, upon which further development of a large interconnected liquid crystal display can build.

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FOR THE FUTURE

The liquid-crystal display is potentially suitable for a wide variety of applications. Fabrication of larger displays, using a modular approach, will make the display suitable for the presentation of television, scan-converted radar, forward-looking infrared (FLIR) imagery, and/or in-raster generated symbology. Integrating the drive circuits using LSI techniques will provide the means for a compact, lightweight, low power display for field-portable installations. The addition of a combiner and suitable optics will make it possible to use the Liquid Crystal Pictorial Display as the image forming device in a high brightness head-up display, and this application is discussed briefly in the following.

HUD Applications

HUDs require display resolution of between 40 to 50 pixels per degree field-of-view. This means that to use the liquid crystal display with current-inventory narrow-to-medium field-of-view HUDs, a total display resolution of between 400 to 800 pixels would be required. Advanced HUDs predicted for future aircraft would require a total resolution capability requirement in the range of 1000 to 1500 pixels to meet the legibility criteria required for their desired wider fields-of-view. The alternatives for obtaining this increased total resolution are increasing the resolution density, increasing the size of the array on a given module, and/or increasing the number of modules.

The feasibility of increasing the resolution density has been examined on a preliminary basis, and it appears that sufficient resolution density can be obtained to meet the total resolution requirement with modules cut from three inch diameter wafers. Hughes has completed a rough "pencil layout" of an elemental cell for a 666 pixel/inch display and computed its dimensional tolerance requirements. While its geometrical dimensions are far tighter than that normally recommended for a very large area device, the cell design, so far, does not indicate the existence of any fundamental problems. Furthermore, the sample-and-hold circuit parameters critical to proper display operation were computed and found to be on par with that being obtained in the present 100-pixel/inch display. This exercise was

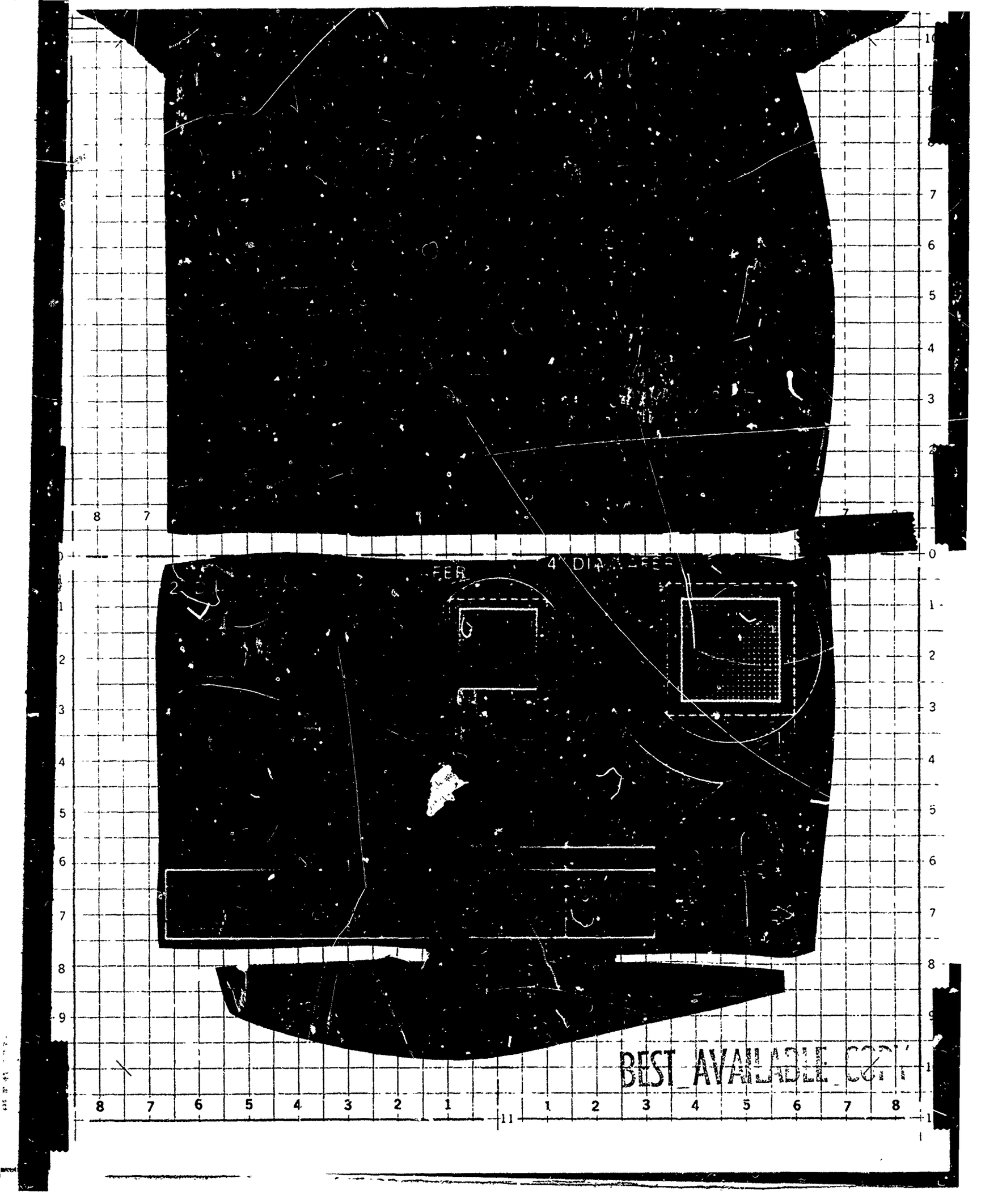
performed only to establish an upper limit; lower density geometries will be correspondingly easier to implement.

The feasibility of increasing the number of modules has also been examined, and it has been concluded that little advantage will be gained by increasing the size of the mosaic array beyond the present 2 x 2-module quad when high density modules are involved. Electrical interconnection at present densities has been shown to be feasible, but the problem of providing electrical interconnection at high conductor densities (several hundred elements per linear inch) appears to be more difficult than increasing the basic resolution density or switching to larger wafers so as to increase the size of the array on a given module.

The impact of increased wafer size on the size of a square display is shown in Figure 17. The switch from two-inch to three-inch wafers has begun on other programs and most all of the equipment required to process three-inch wafers already exists in contractor facilities. The trend in the semiconductor industry is toward even larger wafers, and it has been reported that four-inch diameter silicon wafers are already in production by two semiconductor suppliers.

6 1/2 x 3 3/4

Figure 17. Impact of wafer diameter on size of finished display.


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Advanced HUDs will have to fit within the confines of the forward portion of the windscreen and the upper portion of the instrument panel while not interferring with other structural members. Most important, they must clear the ejection line. In the aggregate, these requirements mean that future increases in the field-of-view for the HUD are more likely to occur horizontally than they will vertically. In reconfiguring a liquid crystal matrix display for Advanced HUD applications, it is possible to take advantage of a rectangular aspect ratio for the field-of-view. For instance, the rectangular layout for the 25:35 aspect ratio shown in Figure 18 reduces the required pixel density by approximately 25 percent by elongating the layout. The dimensions of a quad array constructed from modules so laid out are shown in Figure 19 and Table 1 indicates some of the resolution standards that are to be considered.

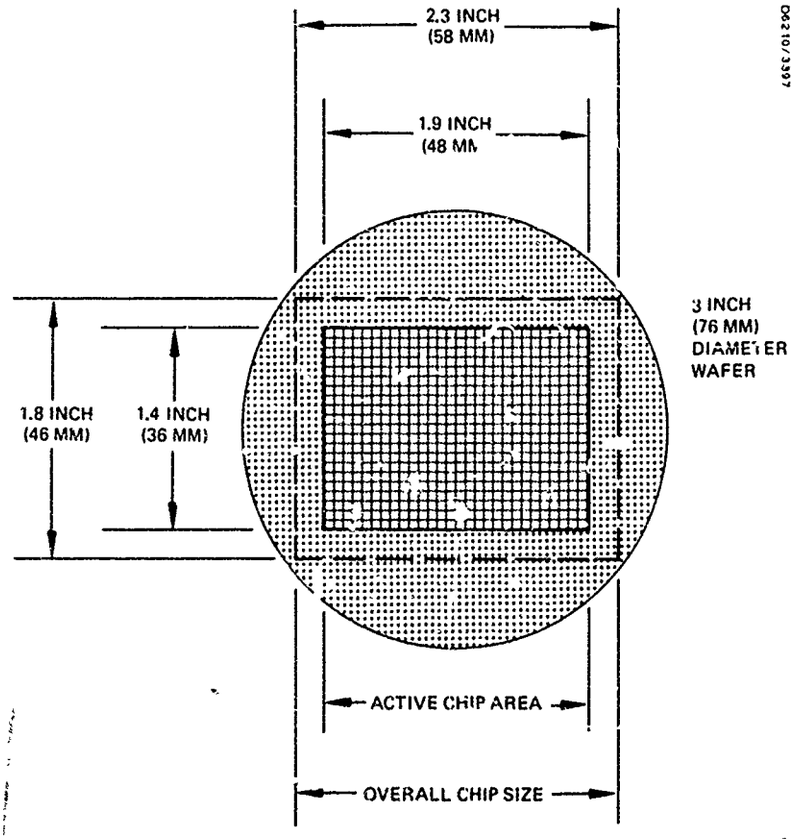


Figure 18. Display chip layout for 25:35 aspect ratio.

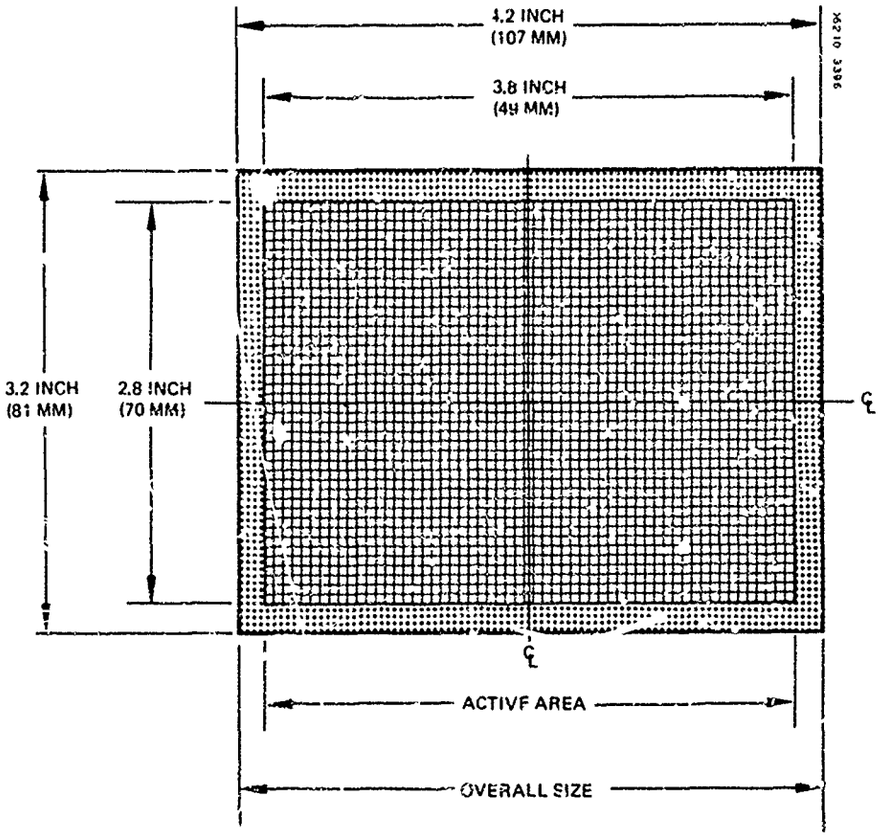


Figure 19. Quad display layout for 25:35 aspect ratio.

In summary, it appears that the higher picture element resolution requirement for the Advanced HUD can be obtained in a quad display by a combination of higher resolution density, display reformatting, and/or larger wafer size.

Use with Holographic Optics

Because the liquid crystal display is reflective over the entire human visual response, it is ideally suited for use in combination with holographic optics, since the hologram optical element has a strongly resolution-dependent sensitivity to the monochromaticness of the illuminant. With the liquid crystal display, the systems designer has the opportunity of optimizing the characteristics of the illuminant (spectral bandwidth and brightness), independent of the display; something that cannot be done with other matrix

TABLE 1

WIDE FOV DISPLAY FORMATS COMPATIBLE WITH STANDARD TV INTERFACES

Total Display Resolution		Resolution Density*
Vertical	Horizontal	
525 line standard (480 active lines)	650	170 pixels/inch 70 pixels/cm 19 pixels/degree
875 line standard (800 active lines)	1100	290 pixels/inch 110 pixels/cm 32 pixels/degree
1029 line standard (950 active lines)	1300	340 pixels/inch 130 pixels/cm 38 pixels/degree
1225 line standard (1100 active lines)	1500	400 pixels/inch 150 pixels/cm 44 pixels/degree

*Assumes 2.8" x 3.8" (7.0 cm x 9.6 cm) display with 25° x 35° FOV.

displays such as LEDs, Plasma and EL Matrices. Even in the CRT, although one can change the phosphor to achieve the desired output wavelength, image quality (resolution and gray-scale) is a strong function of brightness (beam current). Holographic optical elements are expected to play an important role in future HUD designs because their narrow spectral characteristics make them especially well suited for use as the combiner element.

Color

The increasing display of data, even when mode selection has been provided, often results in a cluttered display presentation. The result is that it is particularly difficult to differentiate between categories of moving data when maneuvering. The use of color to code information classes into markedly different hues is an effective demonstrated means of aiding pilot assimilation under these conditions. Unfortunately, the only flyable image-generating color component: the penetration-phosphor CRT would require an order of magnitude improvement in its present light output to be of use in a HUD, although it has been used effectively in commercial aviation panel installations where the display is shielded from direct ambient illumination.

An alternative means of obtaining color in the cockpit would be to use two or more CRTs but this would compound all of the disadvantages of present mechanizations to an impractical degree.

The liquid crystal display can reflect light of any wavelength over the entire visual response and beyond. It becomes possible to take advantage of this characteristic by several means.

- Filtering the pixel elements on an assigned basis with dot or stripe patterns and illuminating the display with broadband light.
- Optically combining two or more matrix displays and illuminating each with an appropriate filtered or narrow-band source corresponding to the desired hue of the color primary.
- Illuminating a single display during each display field with a strobe corresponding to the desired primary hue.

Panel Display

The concept of the large 10-inch square, 1000-by-1000-pixel, liquid crystal television display has been brought closer to reality by the success of the wrap-around rear-bump interconnect technique. The extension of this technique to the fabrication of self-contained modules will make the fabrication of arbitrarily large displays using mosaic array assembly techniques a realistic alternative. It will also facilitate the fabrication of custom display sizes at moderate cost as each new display will only be a reconfiguration of the same basic modules.

The future of liquid crystal panel display is bright because it is unique in its ability to provide a solution to the high-ambient lighting aircraft visibility problem. Undoubtedly, numerous applications will be found for modular liquid crystal television displays as they will be capable of filling a wide variety of needs in much the same manner as the CRT is presently used.

Recommended Development Steps

At the juncture of todays technology, several paths are open for pursuit. These are represented in Figure 20 as possible display configurations. The

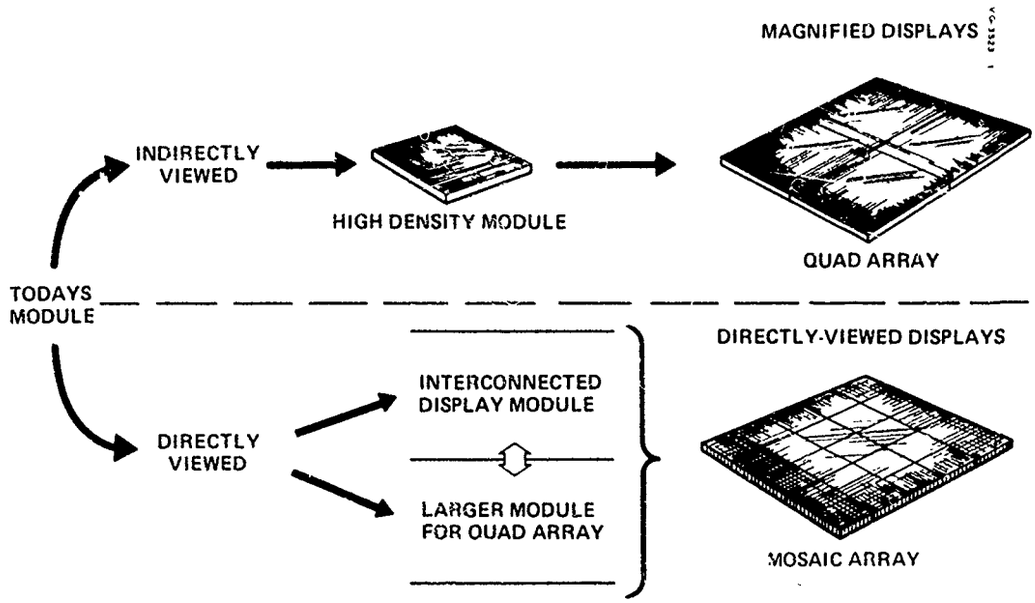


Figure 20. Applicable configurations.

exact course that will be followed is dependent upon future funding and processing trends in the semiconductor industry. Yield as influenced by wafer size and resolution density is an essential part of charting this course and the final choice of wafer size and resolution density selected for production will be determined not only by the display application but by production volume, yield, and cost considerations that cannot be determined absolutely at this time.

The development steps indicated in Figure 21 imply certain basic research and development needs which are itemized in the discussion that follows.

Research and Development Needs

A. Basic Materials Research

1. Synthesize additional nematic, eutectic mixtures for operation in the upper portion of the military temperature range with cell heating to meet airborne military specifications for cold operation.

2. Perform life tests on above.

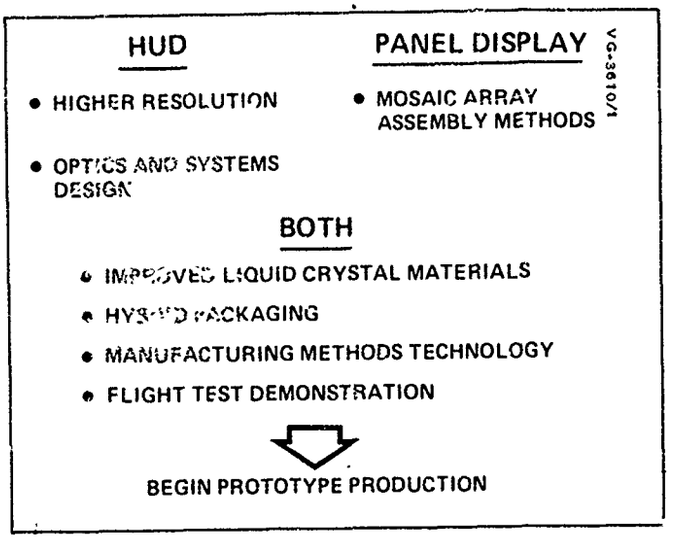


Figure 21. Development steps.

3. Develop improved means of achieving molecular alignment, including a better understanding of surface alignment in general.

4. Perform material compatibility studies of cell assembly and develop filling and sealing procedures that are adaptable to routine production.

B. Semiconductor Display Wafer Development

1. Select a wafer smoothing process and develop a method suitable for routine production.

2. Increase the basic dimension of the wafer to 1.75 x 1.75 in. (4.5 x 4.5 cm) at a resolution density of 128 per in.

3. Increase resolution density to 256 per in., (101 pixels per cm), or other reasonable limit for HUD and for magnified display applications.

4. Develop LSI drive chips compatible with the above including a means for connecting them to the basic display chip or mosaic array.

C. Semiconductor Mosaic Array Assembly Development:

1. Using an operational one-by-module interconnected display as a demonstration vehicle, develop methods for implementing the wrap-around rear-bump interconnect technique that are completely compatible with the electrical and optical operation of the display.
2. Using a three-by-three module interconnect display as a demonstration vehicle, extend the interconnect techniques to an array containing a module that is completely surrounded by other modules, and develop processing/overcoating procedures suitable for hiding the junctions between modules.
3. Develop production processes for sawing, testing, indexing, mounting, and interconnecting modules into completed mosaic displays, and extend the techniques to large mosaic array displays.

Costs

It is difficult to forecast the eventual costs of display subsystems such as the HUDs or panel displays since so much depends upon the specific configuration that is selected for their eventual fabrication and the resultant yields. A point favoring the liquid crystal display is its low device density ($\approx$1600 devices/cm^2) contrasted with routine MOS production which is typically an order of magnitude higher. On this basis alone, good device yields can be predicted for the liquid crystal display. In Table 2, a comparision is presented of the 1 x 1 liquid crystal module with some device densities and yields that have been achieved in the past by the semiconductor industry.

In arriving at yield and cost numbers for the basic wafer, however, it is necessary to look at industry cost and yield data for comparable wafer production and to extrapolate from them. Using wafer processing cost data obtained from complex CMOS and PMOS LSI devices (Figure 22) and yield data from silicon diode array structures (Figure 23) we project the price of a quad display to reach the $5K level. (The silicon vidicon structure was chosen as the comparison device since it has some similarities to the present chip in that it is a large area device.)

TABLE 2

COMPARISON OF LSI DEVICES

Device	Chip Size	No. of Devices	Density of Devices Per Sq. In.	Comment
Sophisticated Desk Calculator	0.2 x 0.3 in 0.06 sq. in Maximum	10,000 to 15,000 15,000	200,000	Production Item
Large Logic Element	0.13 x 0.13 0.02 sq. in	10,000	500,000	Production Item
1024 Bit Shift Register	0.13 x 0.13 in 0.02 sq. in	7,000	35,000	Production Item
4096 Bit RAM	0.23 x 0.23 in 0.05 sq. in	12,000	25,000	American Micro Systems No. 6003
8192 Bit Shift Register	0.170 x 0.180 in x 0.03 sq. in	50,000	1,700,000	Micro System International Toronto, Canada
8192 Bit Dynamic MOS RAM	0.145 x 0.201	9,000	30,000	IBM - 4% Yield After 1st 500 Devices
1000 gate data Communication Chip	$(210 \text{ mil})^2$	2,000 to 4,000	45,000 to 90,000	Signetics (in development)
100 x 100 Liquid Crystal Display	1 x 1 sq. in	10,000	10,000	Experimental

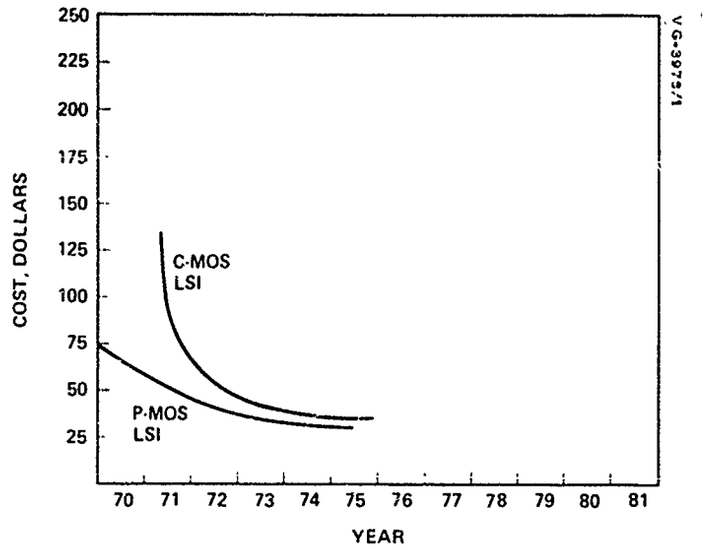


Figure 22. Wafer processing costs.

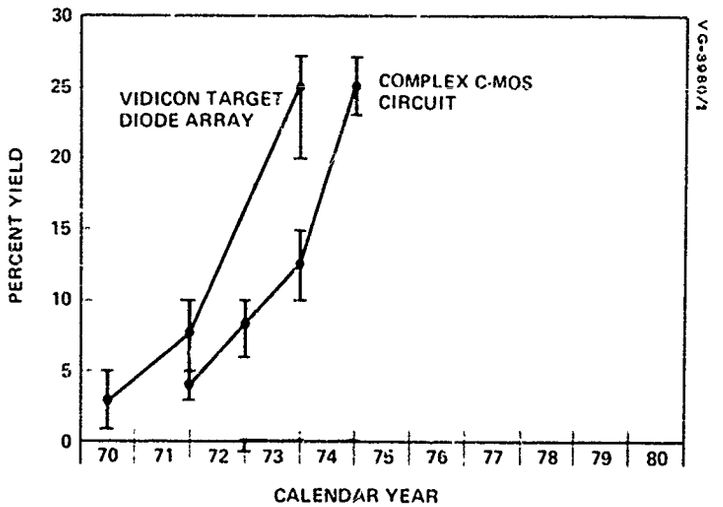


Figure 23. Wafer yield projections.

This computation is based upon moderate or pilot production quantities encountered toward the end of a Manufacturing Methods and Technology (MMT) program where processes are totally under control but production volume is low. Included in this estimate are the anticipated costs and yields of the entire production process, including cutting and assembly labor, the cost of LSI drive circuits, etc.

In Figure 24, the actual cost of the existing quad display and its accompanying discrete component electronics drive is shown for comparison with a small quantity (no production) assembly using LSI drive. In the last example (to the right in the figure) is a completed quad using manufacturing methods and packaging of LSI which are suited to high-volume production, but which are conducted at a modest rate. It is important to note that the latter assembly is in all respects equivalent to a complete television indicator when finished and would be compatible with a standard RS-170 television signal interface.

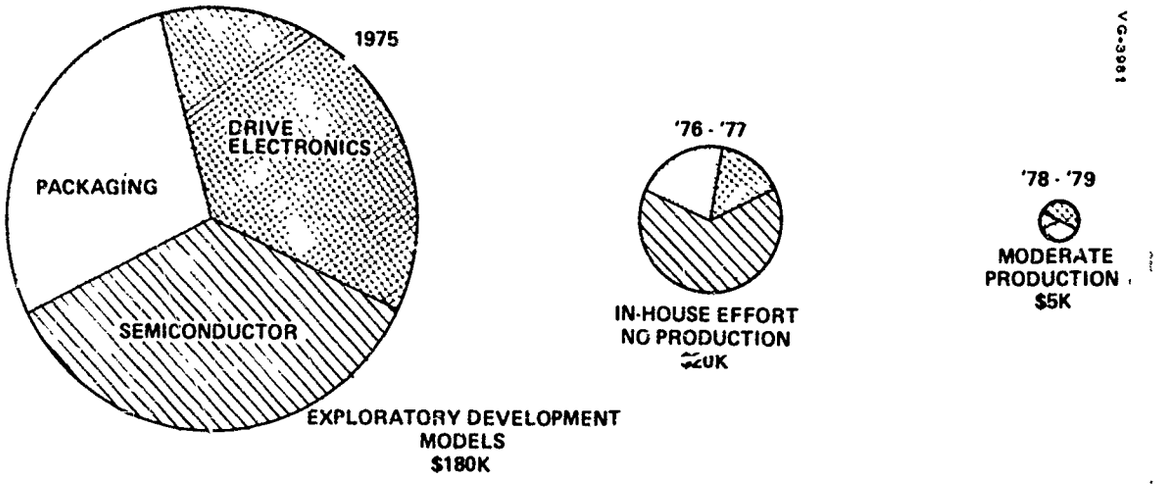


Figure 24. Quad display cost trends.

SECTION II

THE BASIC DISPLAY MODULE AND THE ACHIEVEMENT OF DEFECT-FREE OPERATION

This section reports on the wafer processing and display assembly sequences that were established to build the liquid crystal matrix displays, and the performance level that was ultimately achieved from the display as a subsystem component.

FABRICATION AND ASSEMBLY OVERVIEW

The bulk of the effort in producing a liquid crystal matrix display is processing the semiconductor wafer, from which the chip containing the monolithic array of circuits for addressing each picture element is later cut. This electrode array chip, as either a single unit or in a mosiac of modules, becomes the surface over which a thin-film of liquid crystal material is deposited during the final stages of display assembly. This chapter is concerned with the special processing procedures that are required to produce a line defect free electrode-array chip. The reader is referred to Appendix B if he desires a brief description of the basic wafer processing operations.

Defect Elimination

The circuits for the liquid crystal matrix display are different from traditional large-scale integrated (LSI) circuits: (1) Each wafer yields only one large circuit chip, hence a significant defect anywhere in the matrix array is unacceptable. However, their processing is not especially difficult because the critical areas are small and sparsely spaced. (2) The surface of the finished wafer has an electrode structure which must be of optical quality. Each electrode not only serves as an electrical contact to the liquid crystal material but as an optical mirror as well.

The sequence of processing steps used to produce the wafers for the liquid crystal matrix display consists of those used to produce standard MOS-FET circuits (as discussed in Appendix B) and two additional

steps to produce the reflective electrode structure. Subsequent to the completion of the MOS-FET addressing circuits, a quartz insulation layer is deposited over the polysilicon metalization layer to insulate the addressing circuits from the overlying reflective electrodes. The reflective electrodes are formed by depositing and etching a suitable reflective material such as chromium or silver. The reflective electrodes are electrically connected to the underlying addressing circuits by means of "via" contacts formed through the insulation layer. The entire sequence of processing steps used to fabricate the addressing circuits and reflective electrodes is listed in Table 3.

TABLE 3

WAFER PROCESSING STEP SEQUENCE

1.	p^+ Diffusion	—	Junction formation
2.	Thin oxide grown	—	Gate and capacitor insulator
3.	Contact etched	—	Transistor connections
4.	Polysilicon deposition	—	Metalization layer
5.	Deposit oxide	—	Insulation layer
6.	Via contact etched	—	Electrode connection
7.	Chrome deposition	—	Reflective electrode

Not stated in the table of processing steps but equally important in obtaining a quality device are the conditions under which the specific processes are performed. The wafers for the liquid crystal matrix display are processed in a clean room rated at 10,000 particles per cubic foot. All operations are performed under laminar flow benches such as those shown in Figure 25. The equipment stations under these benches are arranged such that the direction of work flow is from one bench to its adjacent member; a wafer need never be carried across the laboratory outside of closed protective trays. Moreover, special teflon trays are used for all storage and movement of wafers to further minimize the opportunity for contamination.

Automatic wafer handling equipment such as that used with the inspection station shown in Figure 26 is provided for unloading and reloading the special trays.

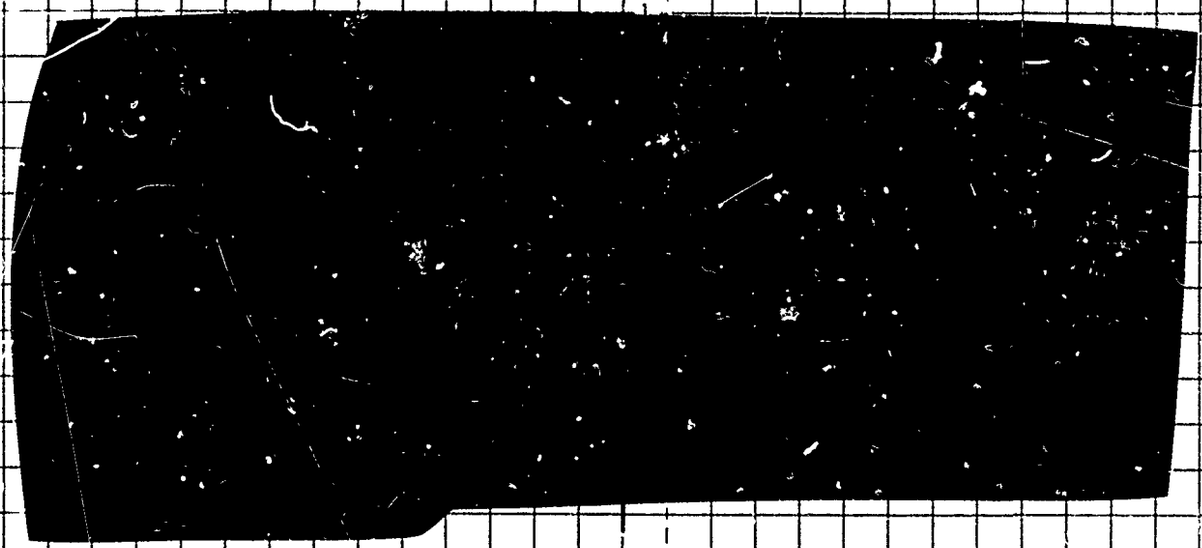
The production of the first "defect free" display represented the achievement of a very high level of craftsmanship in the processing of the wafers, meticulous attention to detail and an optimized design approach. The success of the defect reduction effort can be attributed to four main factors, (1) development of in-process testing procedures that made possible rapid evaluation of results, (2) detection and elimination of mask defects, (3) improved process control and (4) achievement of critical project mass.

Figure 25. Laminar flow-benches.

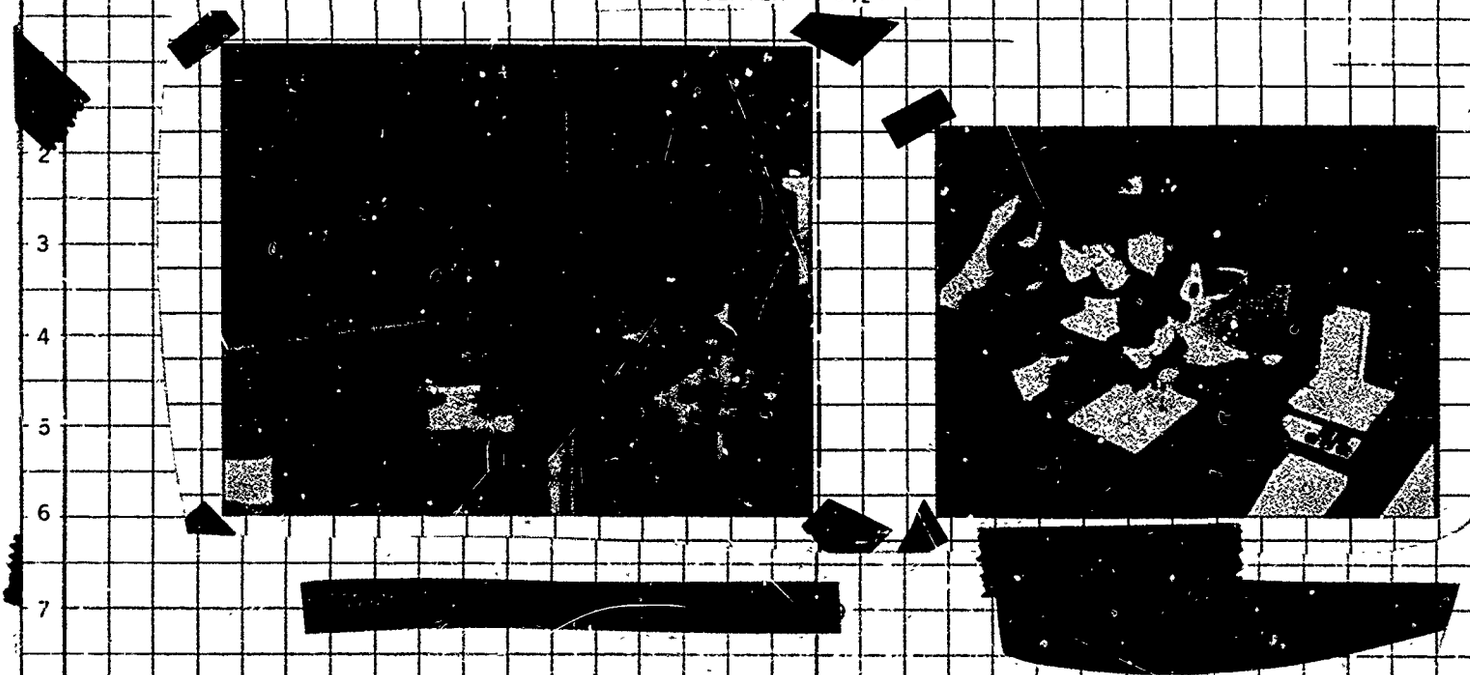
Figure 26. Automatic wafer inspection.

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Early in the program, great difficulty was experienced in trying to establish a cause and effect relationship between fabrication procedures and the quality of the end result. To be able to determine where in the multistep procedure the defects were being introduced, specialized tooling was developed for testing the wafers. An automatic stepping probe station was tried to permit electrical evaluation of the circuits on the wafers immediately after they were completed, but it was found to be too time consuming for a chip having two hundred connections. To speed up the testing, a special one hundred pin probe card and a custom test box was built. Commencement of work on this probe card had been undertaken with hesitation as it required a significant increase in both number and density of probes over that which had previously placed on a single card for testing of semiconductor wafers. The 100 pin card was so effective, however, that no sooner was it received than work was begun on designing a two-hundred pin card that would permit TV testing of the wafers with liquid crystal material; no longer would the devices have to be built up into displays to be fully evaluated. A photograph of the resulting 206 pin probe card is shown in Figure 27. Later in 1975, cleaning procedures were developed that permitted the use of this probe card for an "in-process" test wherein the defect level of the device could be assessed approximately half-way through the semiconductor processing procedure. Figure 28 shows the impact these test procedures had on the time from when a wafer was started until feedback could be obtained on its characteristics. The four to one decrease in test cycle time meant that changes in the processing steps could be iterated at a correspondingly more rapid rate.

In addition to speeding up the testing, the probe cards made it possible to completely test every wafer and not just the most promising devices, so the locations of the defects could be correlated. It soon became evident that

PROGRAM YEAR	TV TEST POINT	TIME FROM START TO TEST
'73	COMPLETED DISPLAY	2 MONTHS
'74	COMPLETED WAFER	1 MONTH
'75	IN PROCESS WAFER (POLYSILICON STEP)	2 WEEKS

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Figure 27. Earlier visual feedback.

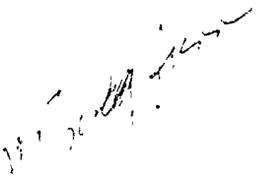


Figure 28. Photograph of wafer M7 #20 on probe station.

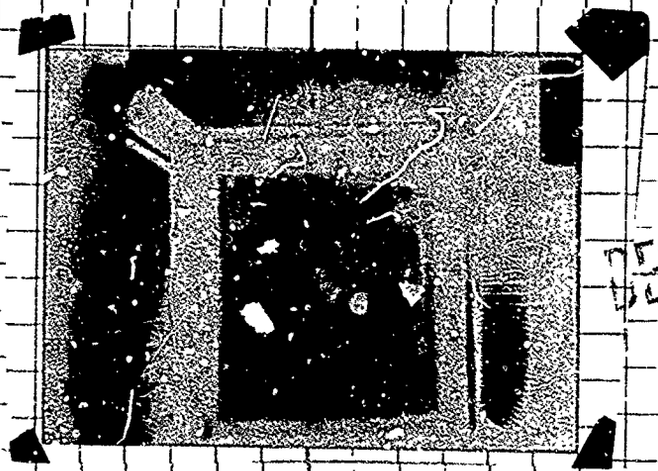
many device defects were occurring repeatedly due to defects in previously unsuspected masks. Figure 29 shows four wafers from lot 95. Careful examination will show that the defects on wafer D95 #18 are also present on one or more of the other wafers. Inasmuch as the probability of a random defect falling on the same line on two different wafers is very small, it can be concluded that wafer D95 #18 would have been defect free had not the masks been defective. Indeed, in almost every case of a repetitive defect, it was possible to trace the wafer defect back to a mask defect (see Figure 30).

At this point in time, the decision was made to move the processing of the semiconductor wafers from the Semiconductor Research Laboratory in Newport Beach to the display production facility in Carlsbad. It was believed, and correctly so, that the program needed a shift in emphasis from process research to production control, and the environment in the display production facility at Carlsbad was more in tune with this shift. The research labs had shown that a defect-free wafer could be produced; it was up to the production facility to accomplish it.

Coinciding with this move, a major program was launched to obtain a defect free mask set. The specifications to which the mask maker was working were carefully reviewed, and a formal procedure for incoming mask inspection was established. Inspection procedures such as the use of a

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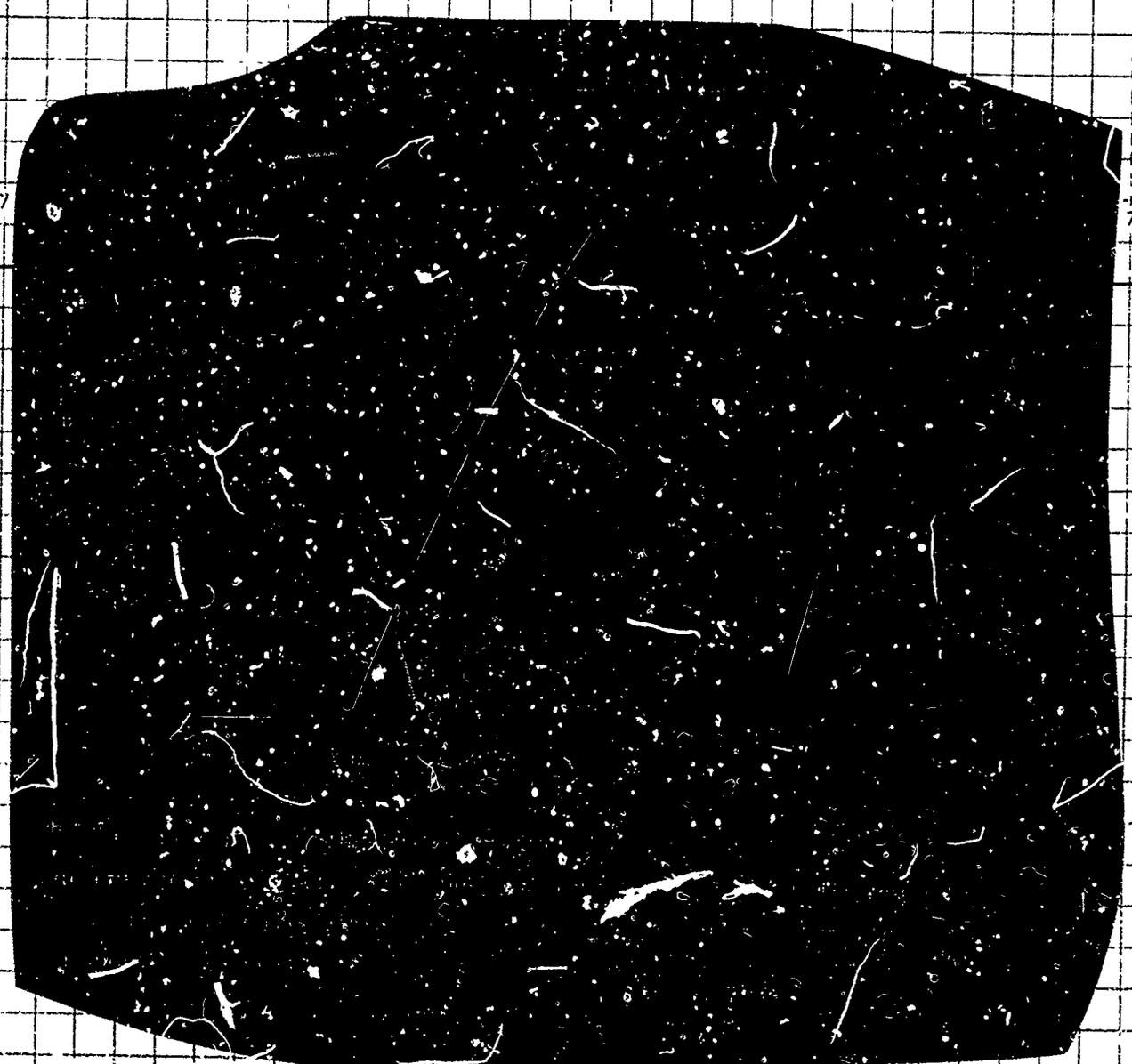
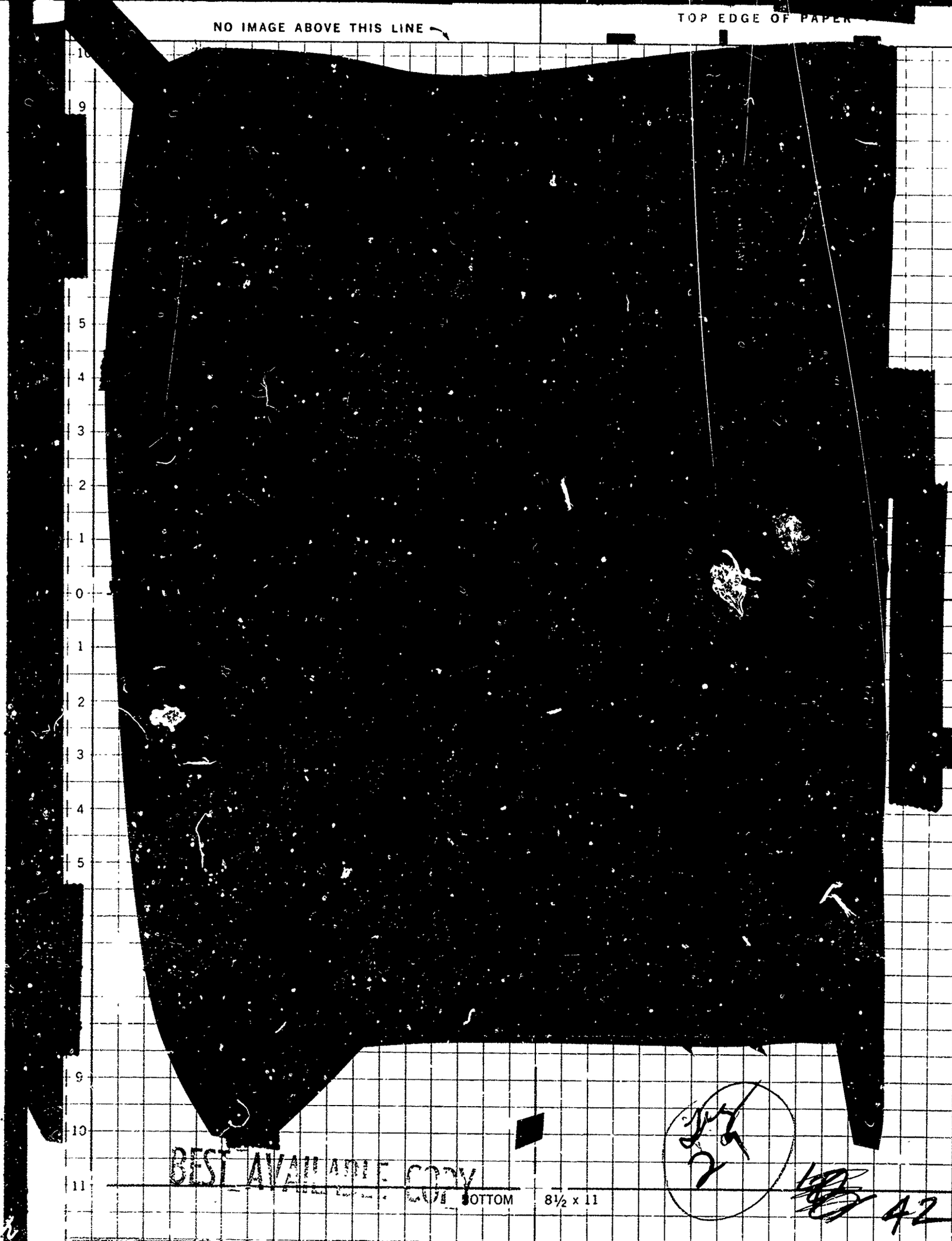




Figure 29. Defects and their cause.

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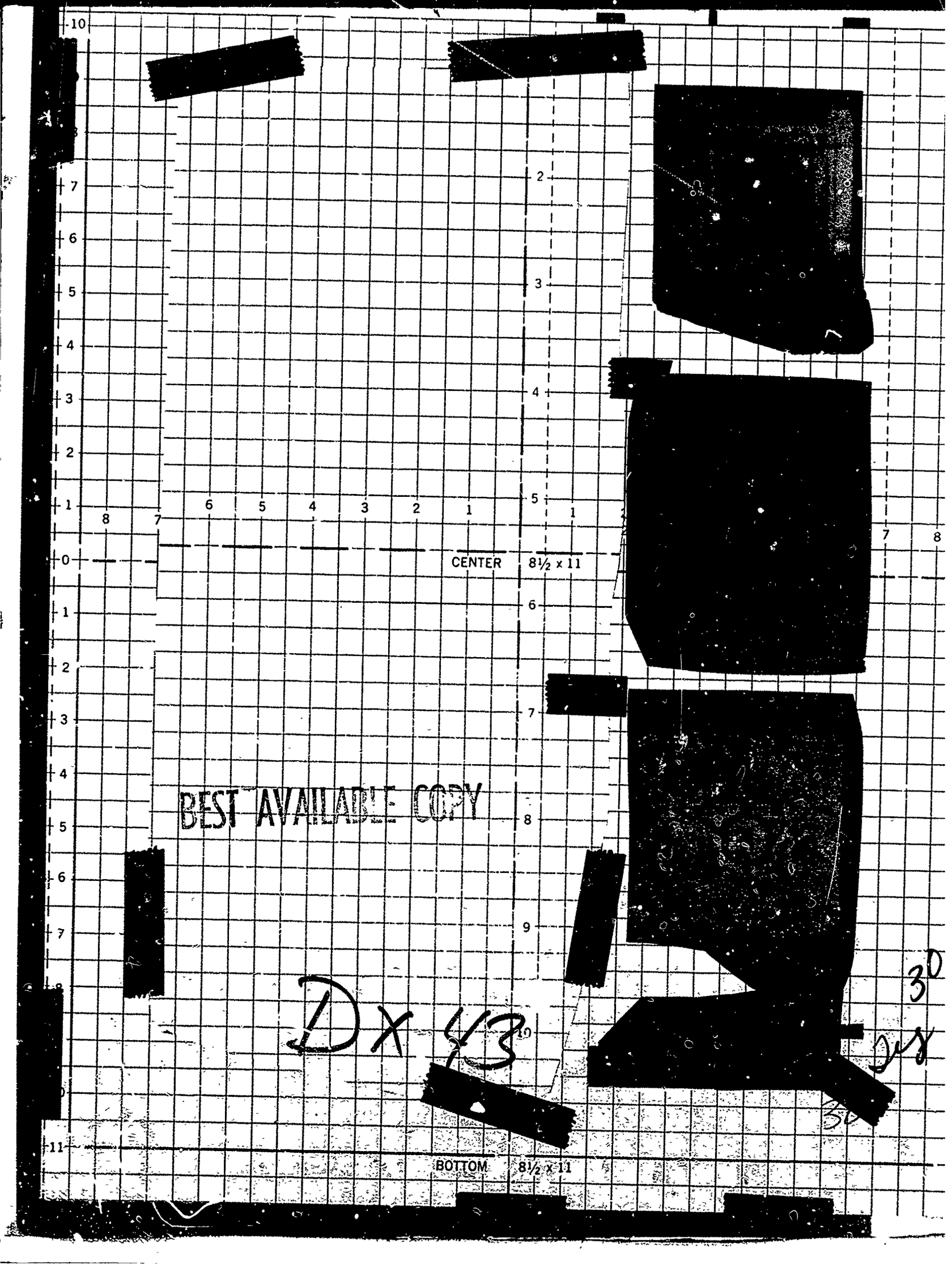
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"student microscope" (which permits two people to look at the same item simultaneously) and an inverted microscope that projects the image on a ground glass were developed to reduce inspector fatigue and improve inspection accuracy. On several occasions, it was believed that a defect free mask set had been obtained, only to find that a particular defect was reoccurring repeatedly due to a mask defect that had been overlooked. The steps taken to eliminate mask induced defects are summarized in Figure 31. As indicated, test data was correlated to locate marginal mask defects that were not obvious from mask inspection alone; routine inspection of the masks was instituted to detect any use-induced defects (scratches, dirt, etc.) on the working masks, and processing procedures such as double-masking were adopted to prevent mask-induced defects where possible.

Simultaneously with the effort to eliminate mask defects an effort was launched to improve control over the semiconductor processing steps. A systems approach was taken toward the examination of the whole process sequence, and steps were added and deleted in an effort to improve the overall yield. The addition of a process step for the purpose of possibly reducing defect was weighed against the probability that a blunder would occur in the execution of that step. Great pains were taken to make the yield at each step as near 100 percent as possible. The photoresist used for the masking operations was filtered immediately before application; the tubes in which critical



Figure 30. Identifying the causes of defects.



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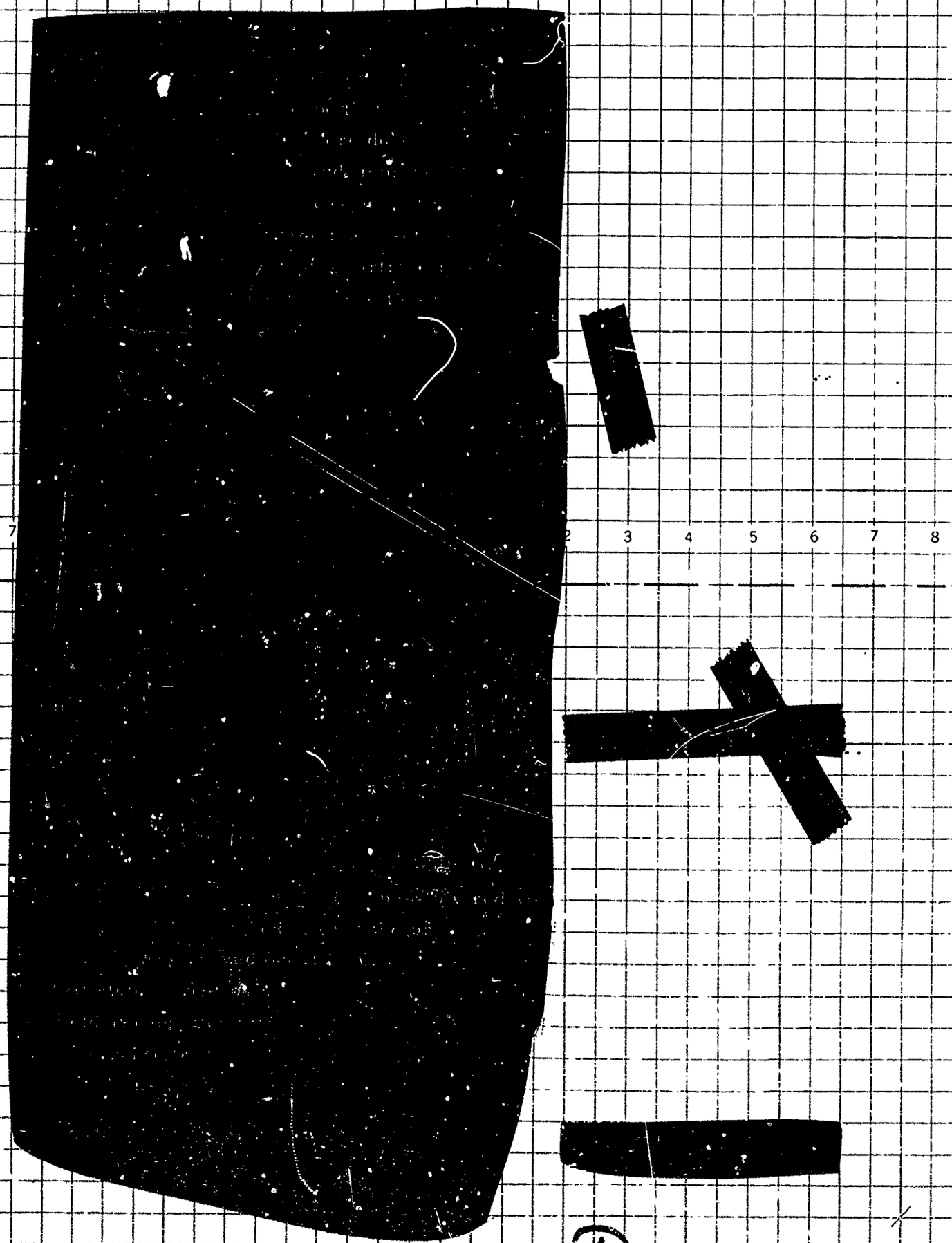


Figure 31. Elimination of mask induced defects.

depositions were performed were cleaned before each run instead of on a calender basis as is standard industry practice; and new deposition techniques were developed, so that the wafers could be placed vertically rather than horizontally during processing to decrease the probability of a particles falling on their surfaces during the deposition operation.

Finally, in June 1975, the line-defect free display shown in Figure 32 was produced. An important factor in achieving defect-free wafer production was the attainment of critical project mass. By critical mass we mean:

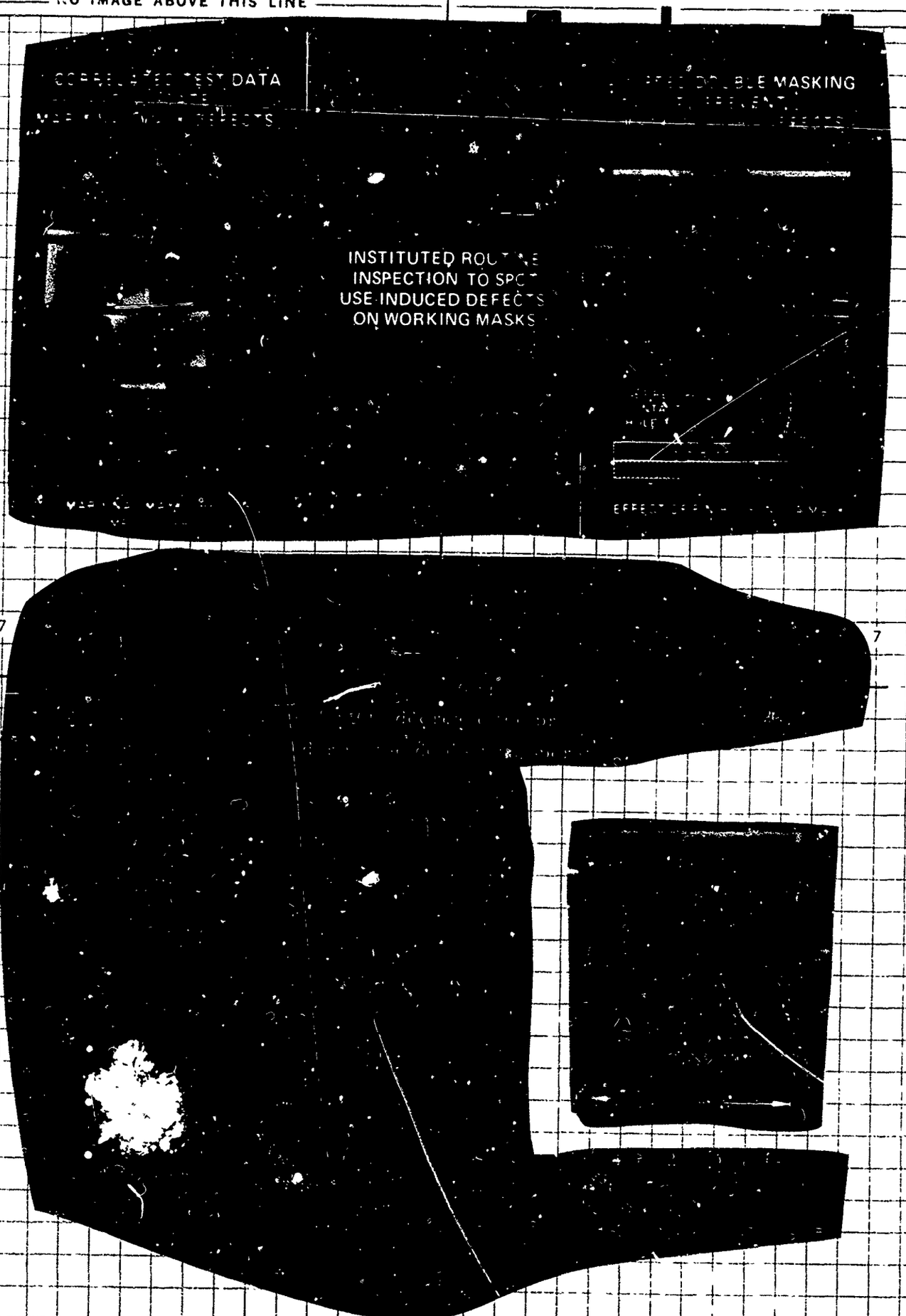
Sufficient production volume to:

- Assure completion of process blocks within a single work day.
- Maintain proficiency of trained personnel.
- Achieve continuity of work flow and thus error free processing.
- Support accurate process monitoring, maintenance personnel, and processing specialists.

Figure 32. Defect-free single module display.

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During the month of June, a quantity of line-defect free devices were produced and stockpiled for later use in the fabrication of the quad displays. The large number of defect free devices and the high yield obtained from the few lots produced during this short time period indicate that the liquid crystal display chip could be produced repeatedly if regular production was maintained.

Final Assembly and Electrical Connection

Display assembly is concerned with taking the silicon wafer at the end of the semiconductor processing sequence and building it into an operational display. The sketches presented in Figure 33 illustrate the assembly steps which are taken at the end of the wafer processing sequence to build an operational display. In the following discussion these are explained in detail.

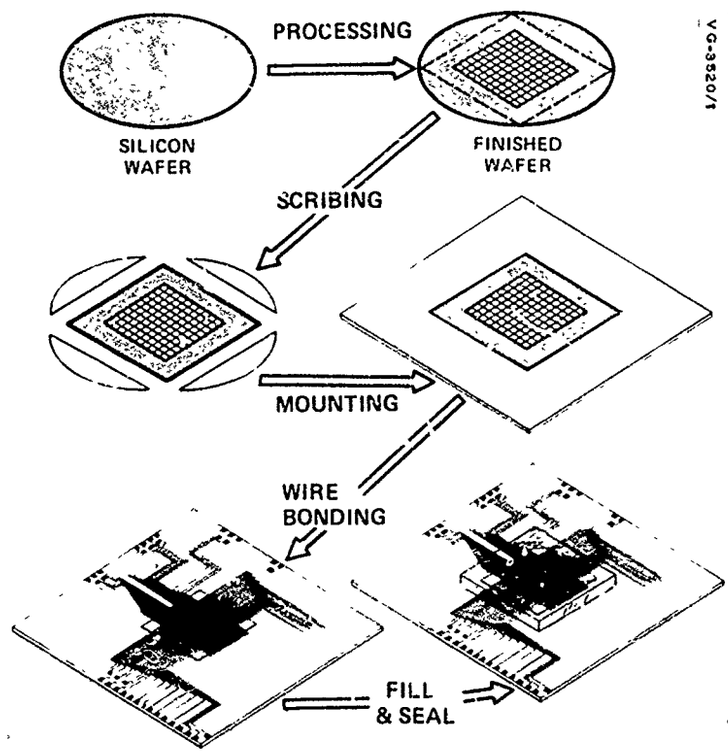


Figure 33. Display cell fabrication.

Scribing

After the wafer processing has been completed, the wafers are cut into the square electrode array chips necessary for the final display. This is done by scribing the wafers on a diamond scribing machine. The wafers are scribed just outside the perimeter of the electrode contact pads, permitting the wafers to be neatly cracked along the scribe line. This provides square chips with the contact pads along each edge.

Mounting

The chips are now ready for mounting to the glass substrate plate. This was originally done using conventional epoxy adhesives, but these were found to cause a certain amount of warpage in the silicon chip as they hardened. A new technique was therefore adopted which makes use of a mylar film coated on each side with a thin layer of thermosetting epoxy. This adhesive is sandwiched between the silicon chip and the glass substrate, and the entire assembly is then placed in an oven and heated to approximately 125°C for a few minutes. This causes the thermosetting epoxy to melt and bonds the silicon chip to the glass substrate. The assembly is cooled slowly to avoid thermal shock, and the mounted display substrate assembly is removed, ready for the wire-bonding operation.

Wire-Bonding

The wire-bonding operation provides connections from the contact pads on the electrode array chips to the corresponding circuit lines on the glass substrate plate. A standard ultrasonic wire-bonding machine is used to fasten thin aluminum wires between the contact pads and the circuit lines. These connections have been found to be quite reliable under the conditions of operation for the present display, although certain precautions have been taken to protect the fragile wires from damage during handling prior to final assembly.

Ion-Beam Etching

The next step in the assembly procedure is ion-beam etching of the electrode array surface to provide alignment for the liquid crystal material.

This is done by placing the display in a vacuum chamber and scanning its surface at an oblique angle with an ion beam. This process produces microscopic "scratches" on the electrode array surface which will control the orientation of the liquid crystal molecules once the display has been filled.

Filling

The filling operation is a process whereby a thin film of liquid crystal material is sandwiched between the electrode array surface and a transparent counterelectrode glass. The thickness of the liquid crystal film is controlled by a mylar spacer placed around the border of the electrode array which supports the counterelectrode at the desired gap. Once the spacer is in place, a small amount of liquid crystal material is spread along one edge of the display surface. As the counterelectrode is lowered into position, the liquid crystal flows across the array surface and fills the gap between the two surfaces. The thickness of the liquid crystal film is nominally 0.5 mil (.0005"). Connection to the conductive surface of the counterelectrode is usually accomplished by means of a thin metal leaf spring or soft indium ball pressed against the inner surface of the counterelectrode.

Sealing

All that remains to complete the assembly of the display is a final sealing operation. This can be done in two ways Displays were originally sealed by flowing a bead of epoxy around the outside edge of the cover glass, which fastened it to the counterelectrode glass. The cover glass extended out past the wire bonds on the substrate plate, provided a good seal and was strong mechanically. Unfortunately, this method was permanent and did not allow the displays to be refilled with new liquid crystal materials. Therefore, a demountable scheme was devised which used an aluminum frame over the cover glass and provided rubber gasket seals. This approach allowed displays to be refilled with new liquid crystal materials for experimental purposes. A photo of a finished demountable display is shown in Figure 34.

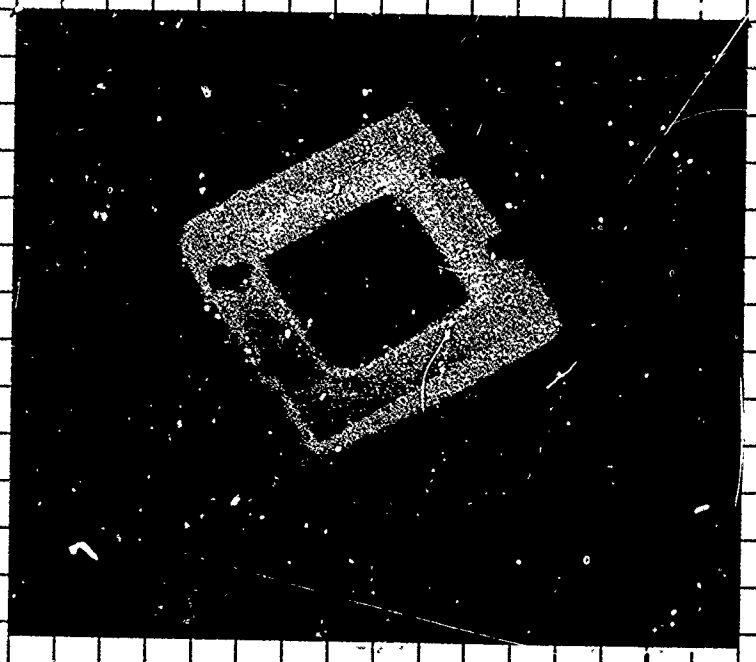
Figure 34. Complete liquid crystal pictorial display cell.

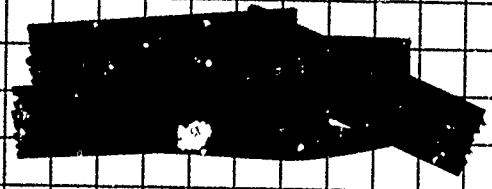
External Display Connections

Connection of the appropriate drive signals to the liquid crystal display is accomplished by means of a special connector that contacts the circuit lines on the display substrate plate. This connector is shown in Figure 35 and 35b. It consists of a glass-epoxy circuit board that fits over the display substrate plate and makes contact to the circuit lines by means of small beryllium copper spring clips. Wires from these clips run to standard ribbon cable connectors on the top of the circuit board. The ribbon cables from the electronics unit plug onto these connectors and provide the driving signals to the display. The connector allows displays to be quickly interchanged without the need to unplug cables or solder new wires.

PERFORMANCE DATA

A liquid crystal pictorial display does not produce light and hence its brightness cannot be expressed in absolute, but only in relative terms. Since the liquid crystal serves as a diffusing media in its dynamic scattering mode, its performance can best be expressed with respect to a perfect diffuser (lambertian surface). The apparent brightness of the liquid crystal will therefore be expressed as a percentage of the comparable brightness of a





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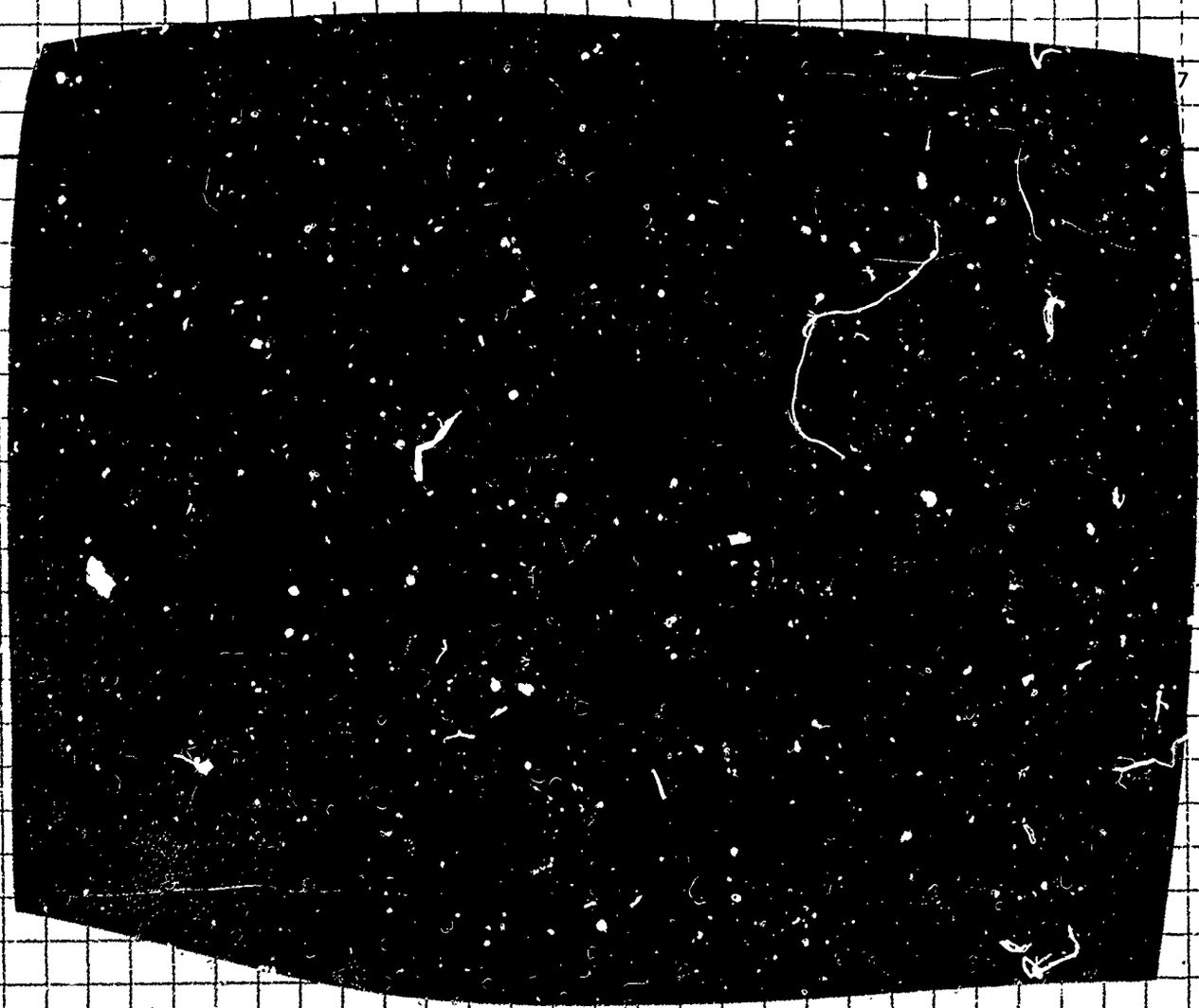
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DX

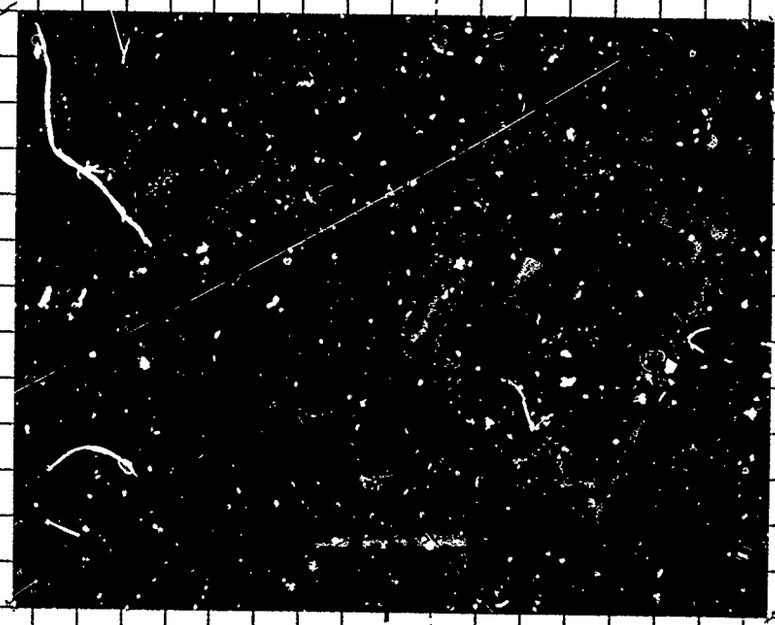
a. Before assembly

b. Assembled with display cell

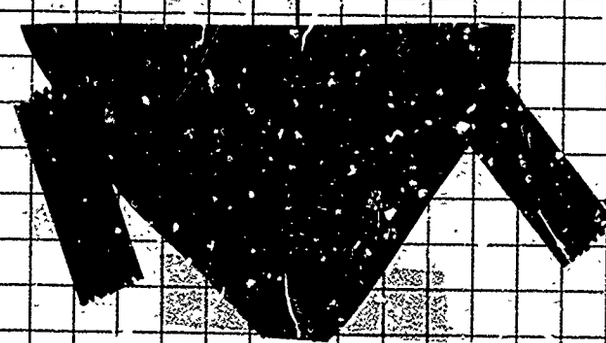
Figure 35 Connector.

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lambertian surface. The brightness of the display is primarily influenced by the efficiency of the reflective electrode in terms of how closely it approximates an ideal mirror. Other parameters, such as surface reflections, and even the liquid crystal itself are of secondary importance. The efficiency of the mirror depends upon its surface material, i.e., chromium, gold, nickel, or silver, and its active area. Non-active areas are not only the gaps between the electrodes, but the areas of the electrode that are not planar with the rest of the display and hence do not contribute to its reflectance. The present electrode material is chromium, which has a handbook value for reflective efficiency of 50 to 60 percent. Measurements on actual displays show that when chromium is used as a reflective material, effective reflectivities of 20 to 30 percent are measured.

The contrast ratio of the display is defined as the ratio of the diffuse reflectance of the display in its "ON" state (dynamic scattering) to its diffuse reflectance in its "OFF" state (background scattering). The contrast of the display depends upon the smoothness of the reflective electrode, the alignment of the liquid crystal material, and on other factors of secondary importance. In present display cells, the reflective electrodes are deposited over the underlying circuit structure and hence the electrode follows this same structure. Tests to determine the significance of these surface irregularities indicate that they are the primary factor limiting contrast. Test wafers constructed with very flat surfaces show dramatic increases in contrast. Contrast of the display is also affected by the alignment of the liquid crystal material. The alignment in typical displays is quite good, but if difficulty is encountered in the filling operation, areas of non-uniform alignment which are visible and degrade the display contrast, may develop.

Present Liquid Crystal Display Performance

Curves showing brightness and contrast as a function of viewing angle are given for a typical chromium display cell in Figure 36. Under normal viewing conditions the brightness of the display is 40 to 100 percent of the brightness of a lambertian surface and the contrast ratio is greater than 15:1. These values are independent of the magnitude of ambient illumination, and it is therefore possible to have a high brightness, high contrast display even in direct sunlight. (See Figure 3, Section 1.) A comparison of a liquid

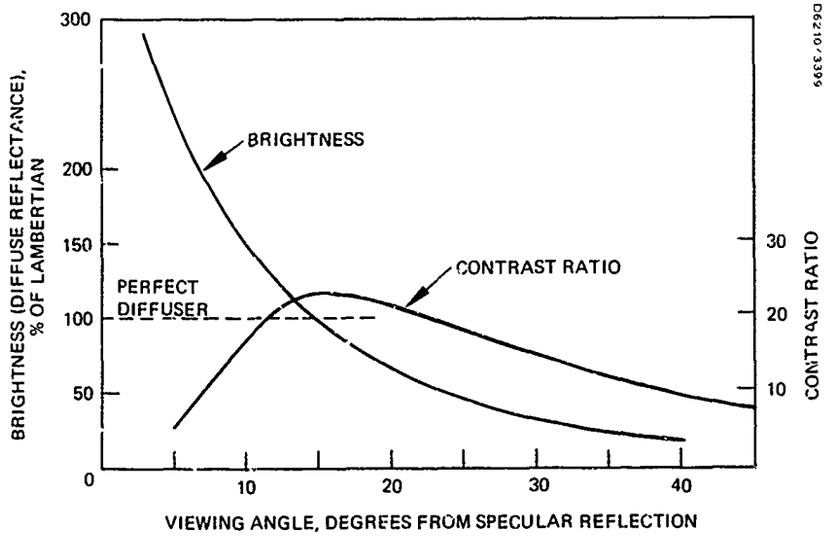


Figure 36. Brightness and contrast versus viewing angle.

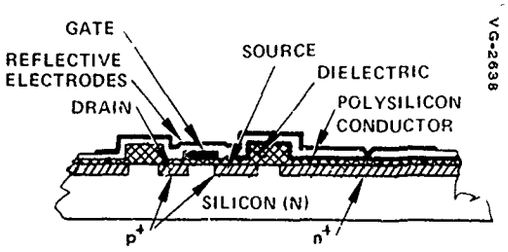
crystal display and a CRT under high brightness conditions is shown in Figure 2, Section 1. Contrast is plotted as a function of viewing angle in a typical cockpit configuration. The liquid crystal display performance is equivalent to that of the best CRTs under 1000 ft-candles illumination, and superior at 10, 000 ft. c. The liquid crystal display is the first technology to permit the presentation of real-time gray-scale imagery under viewing conditions comparable to, and as severe as, those frequently encountered in tactical aircraft operating above the clouds during daylight hours.

Ultimate Limits for Contrast and Brightness

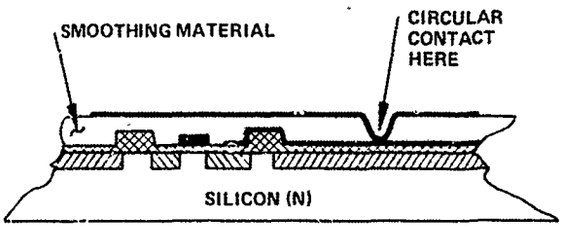
In the future it will be possible to increase both the brightness and contrast of the liquid crystal display. This will be done by changing the reflective characteristics of the display surface. Brightness will be increased by using a higher reflectivity electrode material in place of chromium. Silver has a reflectance approximately 1.4 to 1.8 times that of chromium, and its use will increase the brightness of the display by that factor. Contrast will be increased by reducing the surface irregularities caused by the circuit structure. This will be done by adding a smoothing layer over the circuitry before deposition of the reflective electrode material (see Figure 37). This should increase the contrast ratio considerably. Measurements using smoothed wafers in liquid crystal test cells have shown contrast ratios

greater than 40:1; the results are shown in Table 4. Future display cells should attain nearly equal performance characteristics. The pixel gap which is approximately 0.3 mil (7.6 micrometers) contributes less than 0.5 percent of the background scattering.

In the reflective or dynamic scattering mode the brightness loss, due to the gap, is approximately 6 percent.



a. Existing chip surface



b. Surface under development (with smoothing)

Figure 37. Chip surface before and after smoothing.

Electro-Optic Transfer Curve

The functional dependence of brightness upon the amplitude of the applied driving signal is referred to as the electro-optic transfer curve. Its shape and stability (with time, temperature, viewing angle, and etc.) determines the number of shades of gray that can be reliably presented upon a display. A typical electro-optic transfer curve for a liquid crystal material operating in the dynamic scattering mode is presented in Figure 38. The potential which must be applied before any significant scattering occurs is called the threshold. The potential above which no further increase in scattering occurs is called the saturation potential. The ratio of the saturated scattering level brightness to the background scattering level brightness is the contrast ratio.

The typical threshold voltage for a dynamic scattering liquid crystal material is from three to five volts. For the liquid crystal Pictorial display application, the magnitude of the threshold voltage is unimportant. Whatever its value, it can be offset by applying a fixed dc bias to the counter electrode.

TABLE 4

EFFECTS OF SMOOTHING

	Parameters	% of Lambertian Surface: Existing Surface	% of Lambertian Surface: Smoothed Surface	Comments
Measured Data	Background Scattering of Chip Surface			
	• Random	2	1/2	The X-Y surface structure leads to sharp increases at directions nearly perpendicular to either axis.
	• Horizontal Direction	70	2	
	• Vertical Direction	40	1/2	
	Background Scattering of			
	• Liquid Crystal Material	2	2	12 μm (1/2 mil) thick cell
	Brightness	100	140	Smoothing increases the percentage of planar area and hence increases reflectivity.
	• Narrow Angle Viewing (15°)			
	• Wide Angle Viewing (30°)	25	35	
Anticipated Performance	Contrast (Minimum)	25:1	55:1	
	• Narrow Angle Viewing			
	• Wide Angle Viewing	1:1	10:1	Contrast is angle dependent*

*It is important to note that scattering and brightness data are measured as a percentage of Lambertian, implying that the LX display has gain (directive non-Lambertian) properties; hence it is entirely possible to achieve a 55:1 contrast ratio, whereas if the LX material were truly Lambertian, the contrast would be limited to 40:1 due to the presence of the LX material (2 percent) and the background scattering of the chip surface (1/2 percent).

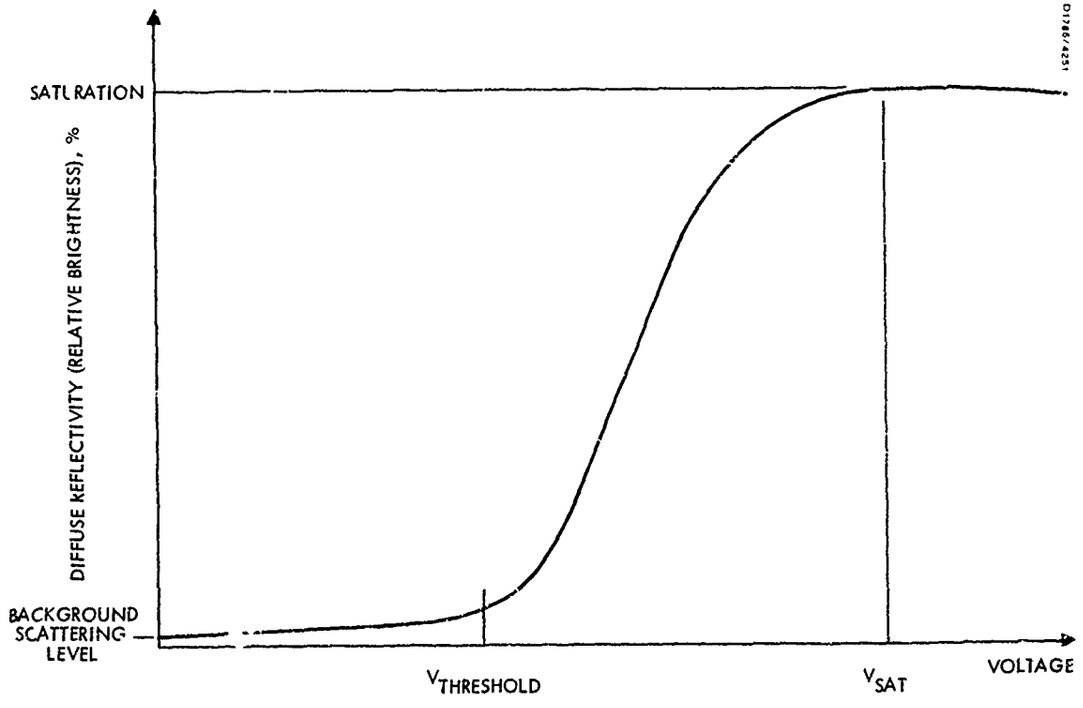
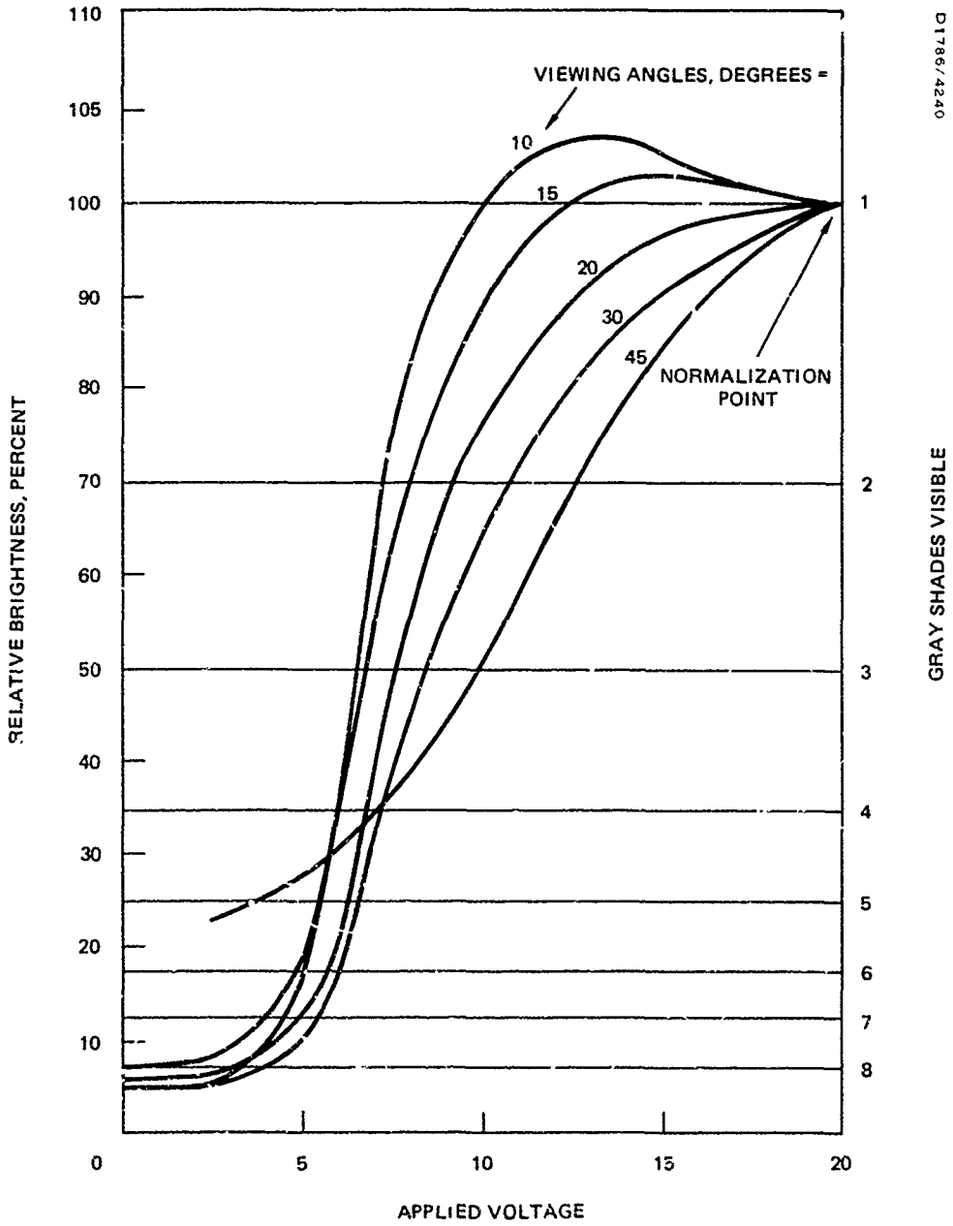


Figure 38. Electro-optic transfer function.

Angle Dependence

Because the display construction employs a scattering medium (the liquid crystal material) placed in front of a mirror like surface, the light scattered by the display will be directional. The light is primarily scattered in a broad lobe close to the angle of specular reflection of the mirror. The exact shape of this lobe depends upon the magnitude of the applied signal.

The net effect on the electro-optic transfer curve is to cause it to shift as a function of viewing angle. Fortunately, the greatest shift occurs at very small and at very large viewing angles, as is shown in the data of Figure 39. For the angles at which the display is typically viewed, there is little change. It is to be pointed out that when the viewer is in the recommended position for viewing the display, he is typically 25° from the normal of the display surface because of the light trapping arrangement. Thus for movement within a head motion box of 15° in azimuth and 5° in elevation, the viewing angle to the display surface varies from a minimum of 20° to a maximum of 34°, centered around 25°.



Note: Data for this figure and others with the light source ⊥ to display surface are correct within ±10 percent for illumination angles up to 45 degrees from ⊥. Viewing angle is then interpreted to be the viewing angle from specular in degrees.

Figure 39. Normalized electro-optic transfer curves.

Speed of Response

Dynamic scattering in the matrix display is proportional to the applied voltage but has a characteristic delay (transport lag) before it exhibits full scattering. This delay time is in the range of milliseconds for typical nematic liquid crystals. The rate of decay in scattering after removal of the applied field depends on the thickness of the crystal, the alignment technique employed and the viscosity of the liquid crystal material. A range from a few milliseconds to seconds can be obtained by appropriate selection of the controlling parameters. Roughly, the decay time varies as the square of the thickness and the square root of the resistivity; it also decreases with increasing temperature.

In defining the speed of response of a liquid crystal cell, the rise time must be distinguished from the fall time, since the two are not entirely dependent on the same factors. The response time, which is not necessarily exponential, is the time required to accomplish 90-percent of the commanded brightness change. For a display that is turned off and on, the rise time is the time required to reach 90-percent of the desired value and the fall time is the time required to reach 10-percent of the previous value. The factors that influence the speed of response of the display are the type of liquid crystal material, molecular alignment, cell thickness, liquid crystal material viscosity, the frequency and magnitude of an ac bias signal (if it is applied), and the resistivity of the liquid crystal material.

Cell Thickness

The decay time of a liquid crystal cell is directly proportional to the square of the cell thickness when parallel alignment is used, as is shown in Figure 40. A decrease in the rise time also occurs which can be explained by the increased electric field when the potential is held constant but the thickness is reduced. The decrease in decay time can be explained in terms of the greater importance played by the surfaces when the volume of the fluid is reduced.

One-half mil or 12 micrometers has been used for cell thickness because that was the thinnest liquid crystal film that could be practically accommodated during early experimental work. The factors of semiconductor warpage, wafer topology, and stress induced factors due to curing of the mounting

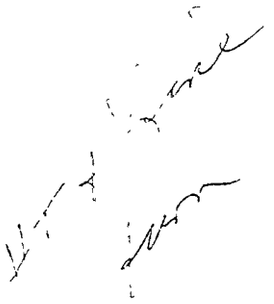


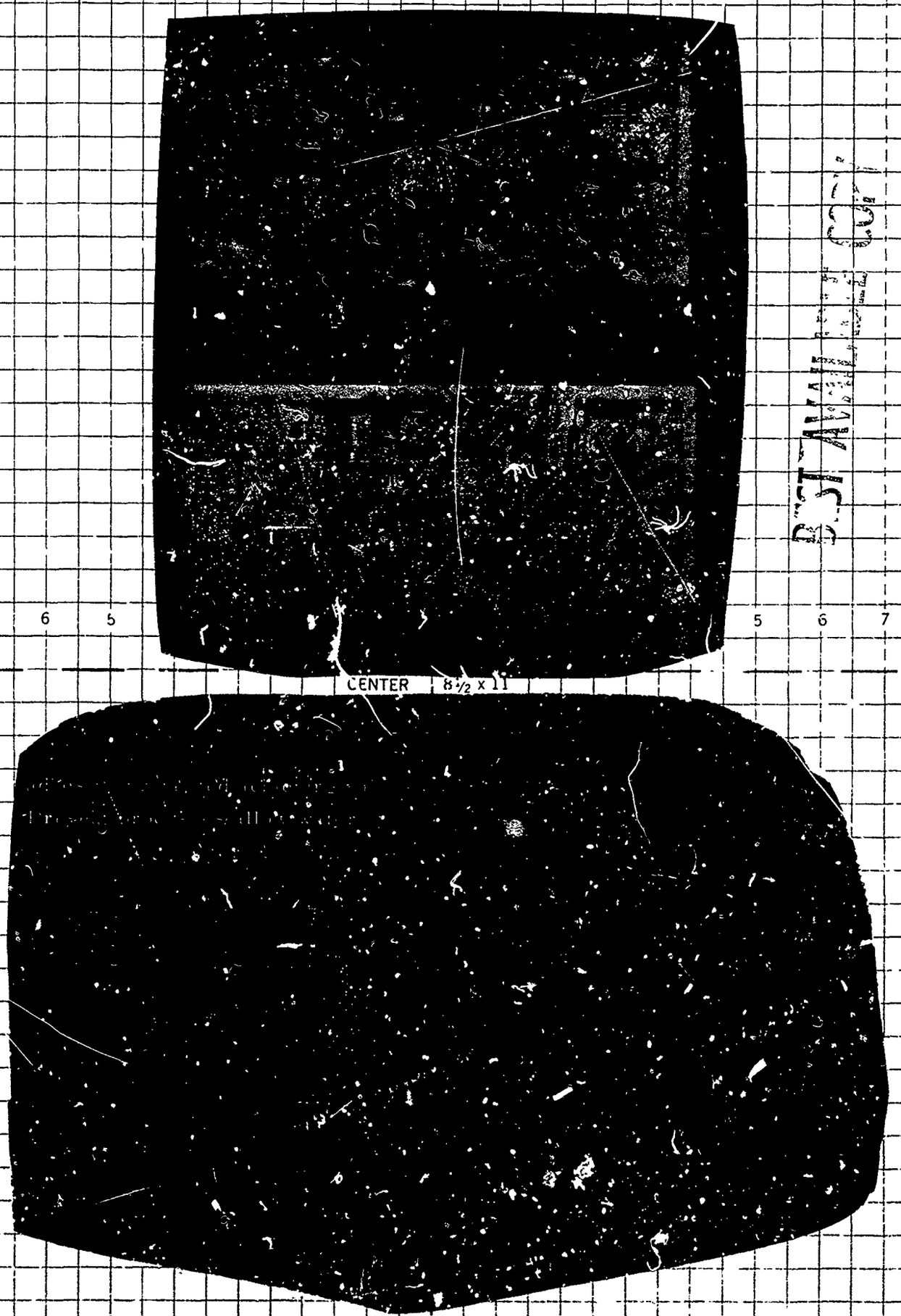
Figure 40. Effect of thickness on observed speed-of-response.

adhesive prevented achieving values that were less than 12 micrometers. Present processes allow wafers to be processed to near optical flatness. New adhesive materials, mounting methods, and final surface smoothing will allow much thinner liquid crystal films and proportionally faster response times. Below 6 micrometers, the contrast ratio with viewing angle is compromised; hence films that are thinner than this value are not recommended.

AC Bias

AC bias decreases the time required for the liquid crystal material to return to the OFF or clear state. Its effect can be predicted qualitatively by examining the dielectric anisotropy of the liquid crystal material at the bias frequency. The effect of AC bias can be regarded as increasing the strength of the parallel alignment mechanism, and thus increasing the speed with

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which the molecules snap back into the parallel orientation. Figure 41 shows an oscillograph of the speed of response of an actual cell with and without bias.

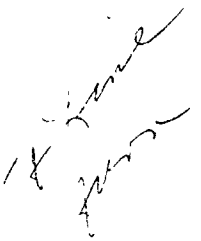
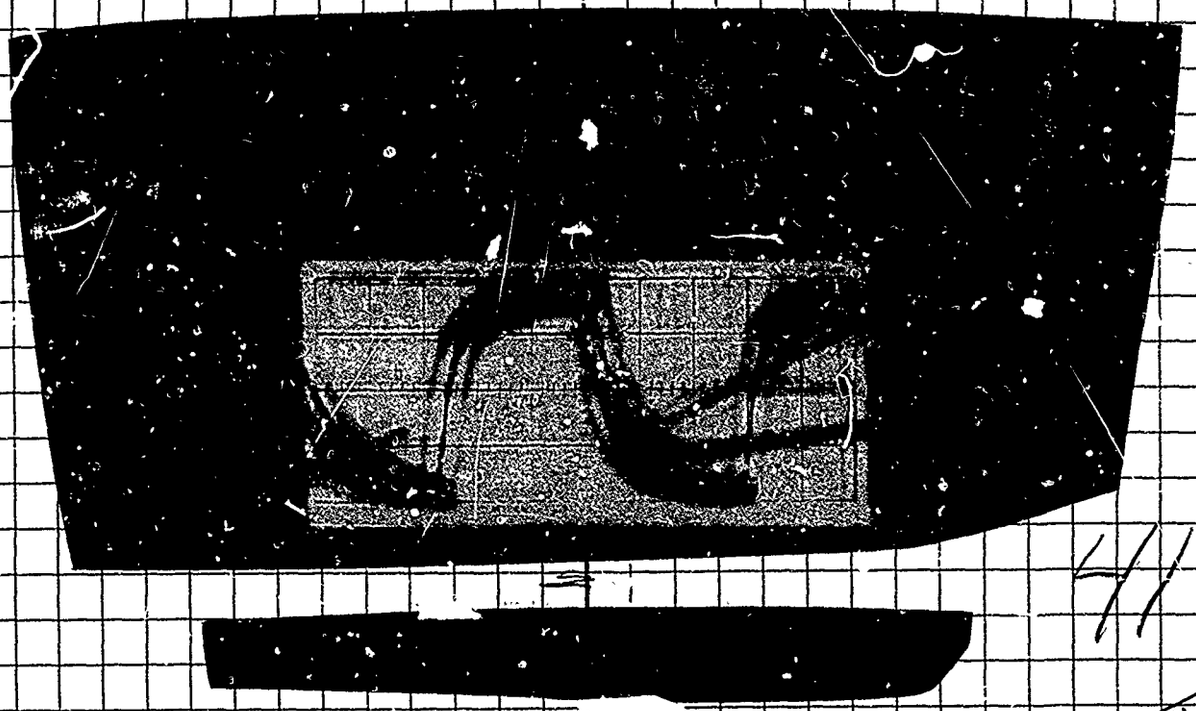


Figure 41. Response time (100 milliseconds/div) (12 micrometer liquid crystal film thickness).

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SECTION III
LIQUID CRYSTAL MATERIAL CHARACTERISTICS

INTRODUCTION

Liquid crystals (LX's) are organic substances and, as the name implies, act like liquids over a specific range of temperature, while retaining some of the properties of crystals. Below the liquid crystal temperature range, the material becomes solid; above this range, it loses its crystalline properties and behaves like a true liquid. In the intermediate liquid crystal range, however, it passes through a turbid liquid state, which is termed the mesomorphic or "liquid crystal" state. The molecular arrangement in the liquid crystal state is more orderly than in the liquid state but less orderly than in the solid state.

The temperature range for the liquid crystal state varies with liquid crystal materials, and considerable effort has been devoted to developing materials which have liquid crystal properties over a wide range of temperatures, including normal room temperature.

What are Liquid Crystals?

Liquid crystals have been classified in three basic categories: nematic, smectic, and cholesteric. The terms denote characteristic spatial configurations assumed by the molecules of these materials. While the molecules of cholesteric LX's are optically active, those of nematic and smectic LX's are generally optically inactive, (i. e., they do not rotate polarized light).

Nematic LX's consist of rod-like molecules aligned in parallel, similar to matches in a box; it is this type of material that is presently used in the Hughes LX display. Each molecule can rotate only around its long axis and has limited freedom of movement from side to side or up and down (Figure 42a). The smectic LX's have a layered arrangement. The layers can slide over one another, because the molecules in each layer can move from side to side or forward and backward but not up and down. Within each layer, molecules may be ordered in ranks (Figure 42b) or randomly distributed. The cholesteric, like the smectic, LX's consist of layers. Within

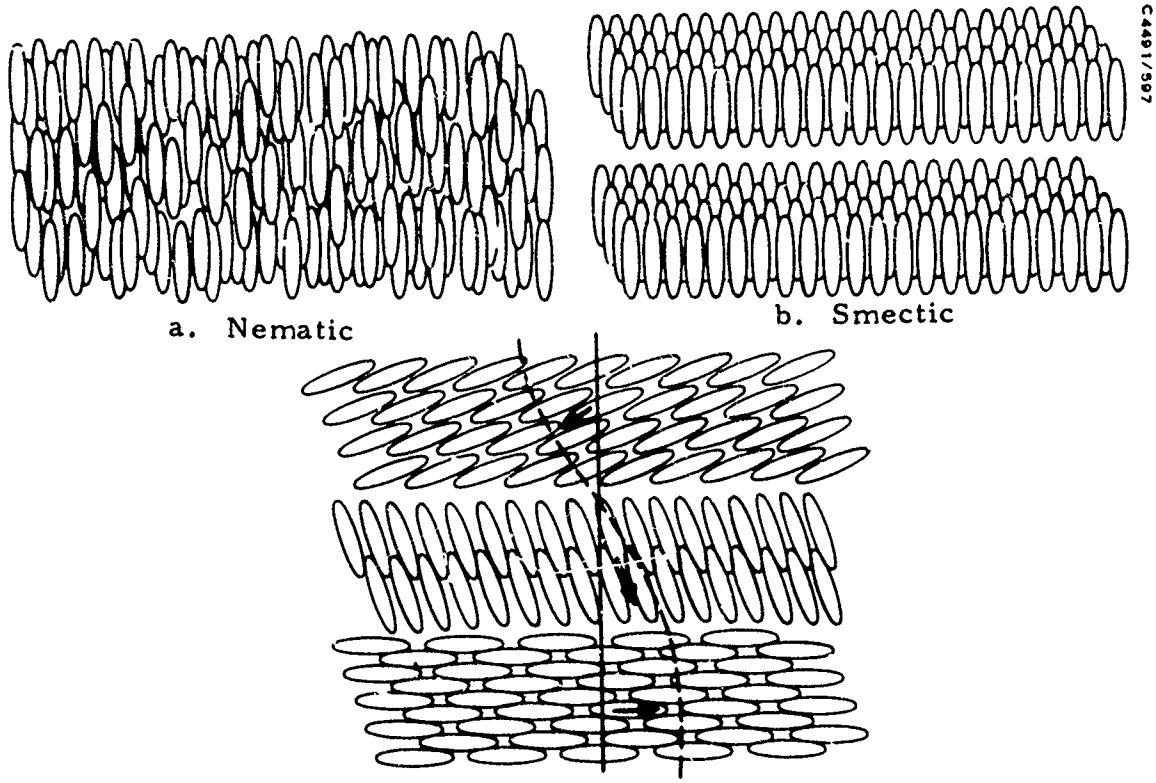


Figure 42. Diagrams of packing effects in liquid crystals.

each layer, however, the molecules are parallel, as are the nematic molecules. Molecules in one layer influence the layers above and below, so that the long axes of the molecules in these layers are displaced slightly and a helical pattern forms from layer to layer (Figure 42c).

A very important property of liquid crystals is the dielectric anisotropy eq. 1, a quantity used to describe the orientation of liquid crystal molecules in the presence of electric fields.

$$\Delta\epsilon = \epsilon_{\parallel} - \epsilon_{\perp} \qquad \text{eq. 1}$$

where:

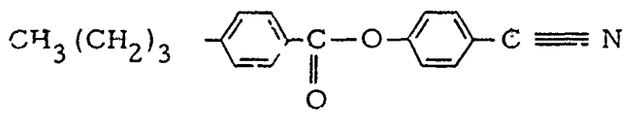
$\epsilon_{\parallel}$ = dielectric permittivity in a direction parallel to the long axis of the LX molecule

$\epsilon_{\perp}$ = dielectric permittivity in a direction perpendicular to the long axis of the molecule

Eq. 1 describes the static dielectric behavior and is most useful in evaluating the molecular behavior or figure of merit for LX materials utilized for display purposes.

In general, when $\Delta\epsilon$ is positive, the molecular axis aligns roughly in the direction of an electric or magnetic field, whereas when $\Delta\epsilon$ is negative, the molecules orient themselves at an angle roughly perpendicular to the field.

The dielectric anisotropy, $\Delta\epsilon$, is a function of the vector sum of the dipolar groups in the molecule. To prepare an LX with a strongly positive $\Delta\epsilon$, for example, it is conventional to introduce the strongly dipolar nitrile group at the end of the long axis of the molecule, as in



Individual properties of each of the types of LX's have been utilized in making displays. The properties associated with each type of LX material are listed below.

NEMATICS:	Dynamic scattering/Field effects
	(1) Twisted Nematic
	(2) Birefringent color switch
	(3) Nematic dichroic dye interaction
CHOLESTERICS:	Reflective color displays
	(1) Temperature sensitive
	(2) Pressure sensitive
	(3) Chemical vapor sensitive
	(4) Electric field sensitive
SMECTICS:	Thermo-optic storage display
HYBRIDS:	Thermo-optic Cholesteric-nematic phase change

Dynamic Scattering Mode (DSM)

Dynamic scattering is a conductivity induced effect which depends upon the dielectric anisotropy of the conductivity doping ions and the optical anisotropy of the nematic liquid crystals The effect of applying a voltage across a typical LX cell is to induce hydrodynamic motion (see Figure 43) which disrupts the normally uniform molecular orientation in favor of a large

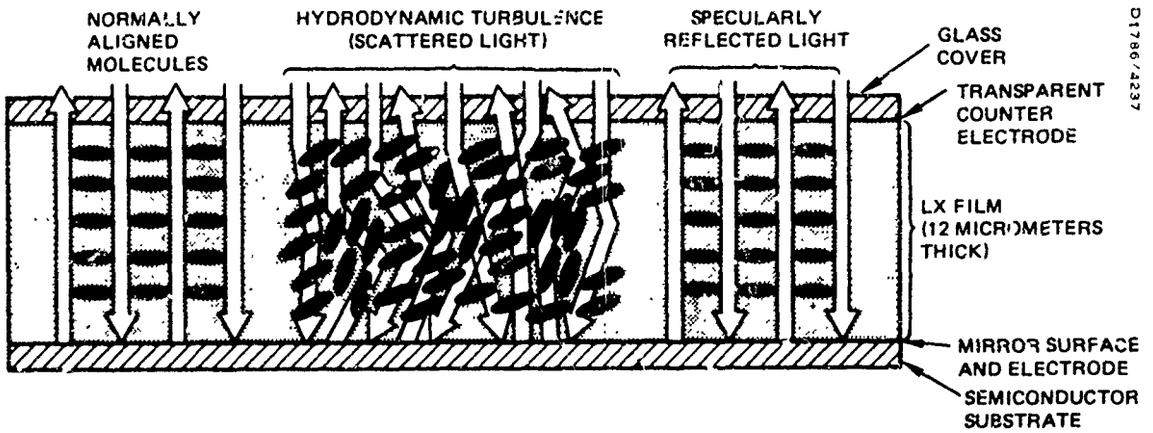


Figure 43. Nematic LX shown in dynamic scattering mode (DSM).

number of small regions (domains) whose molecular orientation is different from those of their neighboring domains. The effect on light passing through the cell is that of closely spaced refractive index boundaries. These index boundaries refract the light at various angles (i.e., scatter it). The result is a system that is optically homogeneous and transparent when no voltage is applied and highly diffusing or scattering when voltage is applied.

DSM can be activated by either AC or DC signals. When AC is used, the frequencies are typically less than 1 KHz. The voltage value is dependent upon the material constituency and classification and ranges from 0.5 volt to 60 volts. In the Hughes LX matrix display, the excitation is unipolar and of varying amplitude (22 volts or less) depending upon video scene content. An AC bias of 60 volts peak to peak amplitude and appropriate frequency (depending upon material constituency) helps return the molecules to their normally aligned state after the excitation is removed.

Field Effect Mode

Another way to take advantage of the sympathetic alignment and the optical anisotropy of nematics is the twisted nematic configuration shown in Figure 44. The design of the twisted nematic cell is the same as for the DSM, except that polarizers are required and the cell walls are treated to make long axes of the LX's parallel to the plane of the cell wall. As a result, on each cell wall the long axes of the LX molecules are parallel to each

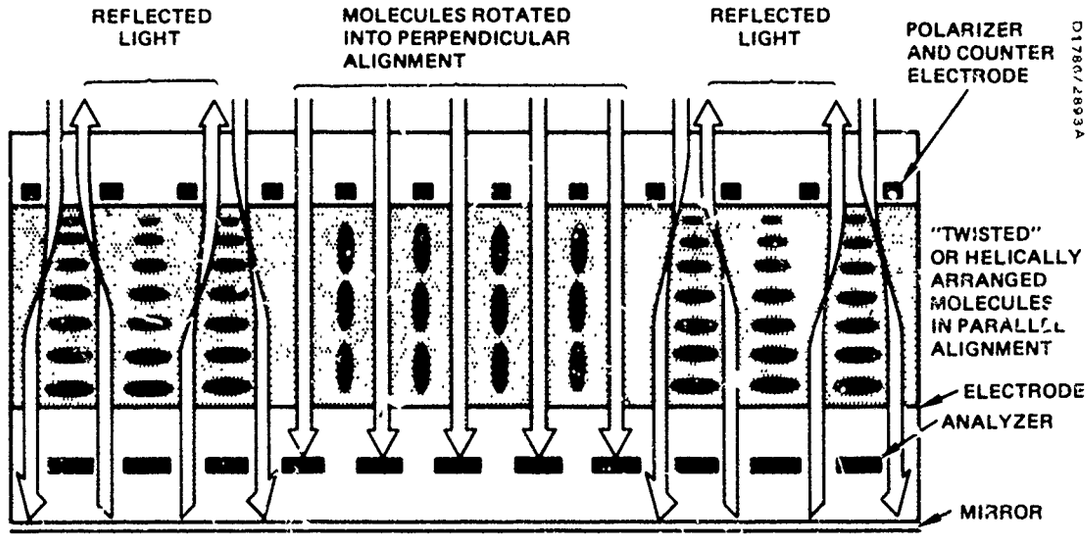


Figure 44. Twisted nematic LX shown in field effect mode.

other as well as to the plane of the cell wall. The cell is assembled to form an angle of 90° between the direction of the long axes of the LX's on one wall and the corresponding direction on the other wall. Calculations show that the orientation of the long axes of the molecules varies smoothly across the cell thickness from one orientation to the other. Hence, the name twisted nematic.

If light incident on the cell is plane polarized either along the direction parallel to the long molecular axis or perpendicular to it, the plane of polarization of the light emerging from the other side of the LX cell is rotated 90°. When viewed through a polarizer oriented normal to the analyzer, this emerging light is observed to pass through the polarizer. However, if a field of sufficient strength (typically a few volts) is applied to the cell, light is blocked by the analyzer. The reason is that the molecules in the bulk change their alignment with the cell wall from parallel to perpendicular. As a result, no rotation of the plane of polarization of the light occurs when the field is applied. Since the analyzer is aligned normal to the polarizer, light is now blocked. Thus, by using a linear polarizer and analyzer in conjunction with a twisted nematic configuration, the intensity of the transmitted (polarized) light can be modulated with an electric field; hence the term "field effect," as opposed to DSM which is a current induced effect.

In their present state of development, nematic materials operated in the dynamic scattering mode, offer the most promising application to the matrix display technique described in this report. However field effect operation would be equally desirable if there were a practical method of applying a polarizer to the reflective surface of the matrix display substrate.

Implications on Viewing

The requirements for an illumination and viewing system using a liquid crystal display are largely determined by the optical characteristics of the liquid crystal being used: field effect or dynamic scattering.

Field-Effect Materials

Field-effect liquid crystal materials rotate the polarization plane of the light passing through them. To take advantage of this rotation in display devices, polarizing filters are required to present contrast. Thus, there is an inherent light loss of over 59 percent due to these filters alone, and the overall efficiency of the optical system is reduced. In cockpit applications it is often necessary to have an extremely bright display in order to maintain contrast against the high ambient lighting conditions. The use of polarizers in the optical system would therefore require increased output from the lighting system and hence larger input power requirements. The use of field effect materials is therefore considered undesirable for cockpit applications.

Dynamic Scattering Materials

In viewing a liquid crystal display utilizing dynamic scattering material, the liquid crystal in its quiescent state is transparent and any light striking the display will specularly reflect off the mirror surface. When the liquid crystal is excited into its scattering mode, some of the incident light will be scattered at angles other than at the angle of specular reflection. This scattered light takes the form of a lobe centered around the specular reflection, as shown in Figure 45. The size and shape of this lobe is dependent on the voltage applied to the liquid crystal. As the voltage is increased, the lobe becomes broader and more light is scattered over a wider angle. The liquid crystal is therefore acting as light modulator by scattering light in proportion

to the voltage applied to it. The brightness of the display is proportional to the intensity of the incide ' illumination, and its brightness therefore expressed as a percentage, using the brightness of a lambertian surface (a perfect diffuser) as 100 percent, as discussed previously in conjunction with Figure 35. Both brightness and contrast are a function of the viewing angle relative to the specular reflection. The contrast reaches its maximum at viewing angles between 10^{o} and 15^{o} from the specular reflection, and decreases as the angle becomes smaller. This is due to dispersion and scattering that occur at narrow angles off the display surface and the liquid crystal. The illumination and viewing system should therefore be constructed to use as much of the scattered light as possible, while avoiding the light scattered at narrow angles from undesired sources.

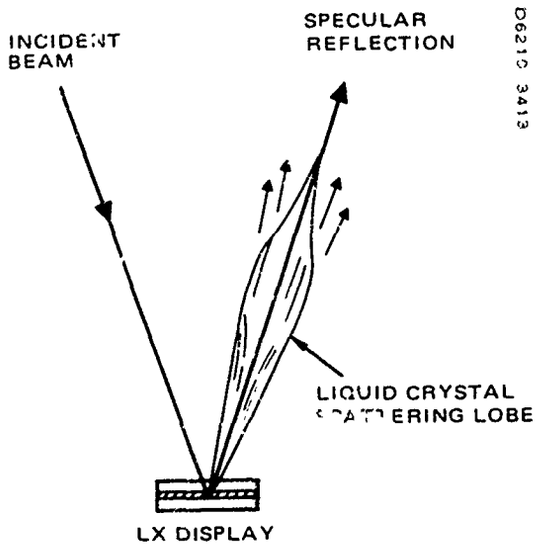


Figure 45. Liquid crystal scattering lobe.

LIFETIME

Sample test data indicates that a Liquid Crystal Airborne Display can be expected to have long operational and storage lifetimes provided the display is properly designed, assembled, and operated. Admittedly, a great deal of work remains to be done to determine why certain displays prematurely fail, but the fact that several have continued to operate indicates that the problems are not insurmountable. Long operational lifetimes are observed when the displays are assembled using a compatible combination of materials, and operated with electrical signals of the correct magnitude and polarity. Long shelf lifetimes are observed when the selected liquid crystal material is a precise eutectic solution, of very high purity, and protected from the entry of contaminating materials.

The key factor responsible for the long operational lifetime of the liquid crystal airborne display is the use of redox dopants in the liquid crystal material. Redox dopants effectively neutralize the undesirable electrochemical reactions that take place on the electrode surfaces, by providing electron donors and acceptors that (1) form at lower electrochemical

potentials than the decomposition potentials of the liquid crystal base material and (2) exchange their donated or accepted charge, after migration to the opposite electrode, in a completely reversible manner. Slight imbalances in the relative concentrations of donors and acceptors are accommodated by the migration of the excess carrier toward the opposite electrode where its complementary carrier is present in an equal amount.

The key factor in extending the shelf life of the present liquid crystal airborne displays has been the use of Ester-based as opposed to the more conventional Shiff-based liquid crystal materials. Schiff-base materials are advantageous because they are available in a wider range of formulations and at lower prices than Ester materials as a result of being the material used in liquid crystal digital wrist watches. However, the present cells use epoxy materials as part of the peripheral seal, for ease of assembly, and their porosity with respect to water vapor makes the use of the hydroscopic Schiff-base materials inappropriate. Ester-based materials have a longer shelf life because they are far less sensitive to contamination by water. Obtaining the same shelf life with a Schiff base material would require developing the necessary glass kit sealing techniques. This does not preclude the use of Schiff-base materials at some time in the future.

TABLE 5

SOME EXPERIMENTAL, EXTENDED-RANGE LIQUID CRYSTAL MATERIALS

Mixture	No. Components	Eutectic	Nematic Range, Centigrade	Dielectric Anisotropy
Old				
HRL-2N10	4	No	20° to 55°	-0.12
HRL-2N12	5	No	14° to 55°	-0.25
New (Experimental)				
HRL-2N14-X	3	Yes	3° to 56°	-0.40
HRL-2N16-X	5	Yes	-12° to 56°	-
HRL-2N20-X	4	Yes	18° to 82°	-0.56
HRL-2N21-X	3	Yes	16° to 78°	-
HRL-2N22-X	5	Yes	12° to 55°	-0.78

The exact end of life for a liquid crystal display is difficult to determine because there is not catastrophic failure. In most cases there is a gradual reduction in the contrast ratio, and in some cases, small inoperative regions develop where gases formed by electrochemical reactions with contaminants push the liquid crystal material away from the electrode structure. In the life test performed by Hughes, end of life was defined as either a factor of ten decrease in the resistivity of the liquid crystal material or the formation of a gas bubble large enough to be seen by the unaided human eye. In the liquid crystal airborne display the resistivity is a particularly important parameter as it directly affects the brightness and contrast of the display. A liquid crystal material with too high a resistivity will not scatter light well, and a liquid crystal material with too low a resistivity will discharge the elemental storage capacitor before a significant level of scattering is established.

To provide lifetime data on the liquid crystal material being used in the Liquid Crystal Airborne Display, test cells were fabricated, operated continuously, and monitored for changes in resistivity. The data in Figure 46 shows that lifetimes well in excess of 10,000 hours can be achieved.

RESPONSE CHARACTERISTICS

Speed-of-response of the present display has been discussed earlier in Chapter 2. The chief liquid crystal material factors affecting turn-on and turn-off times will now be discussed.

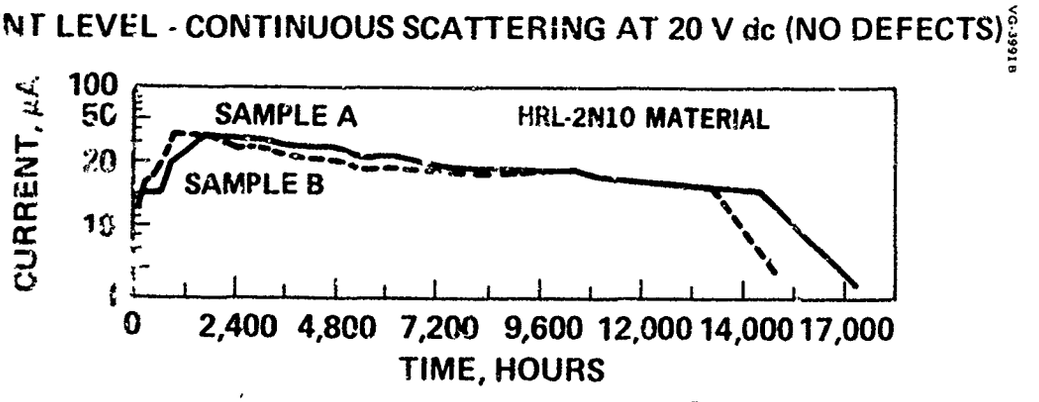


Figure 46. Lifetime test data, DC dynamic scattering.

Alignment

The liquid crystal material molecules can be oriented with their long axes either parallel or perpendicular to the plane of the electrodes. The speed of response of the display depends on the orientation selected, as is shown in Figure 47. With 1/2-mil thick cells, such as the present display cells, perpendicular alignment yields a faster rise time but a slower fall time. Parallel alignment was selected because decreasing the fall time by several hundred milliseconds was considered more important than decreasing the rise time by only a few tens of milliseconds.

Viscosity

The response time of a liquid crystal material is typically represented by the equation[3]:

$$t = \frac{C\eta}{\epsilon E^2} \qquad \text{eq. 2}$$

where

C = Constant

η = viscosity

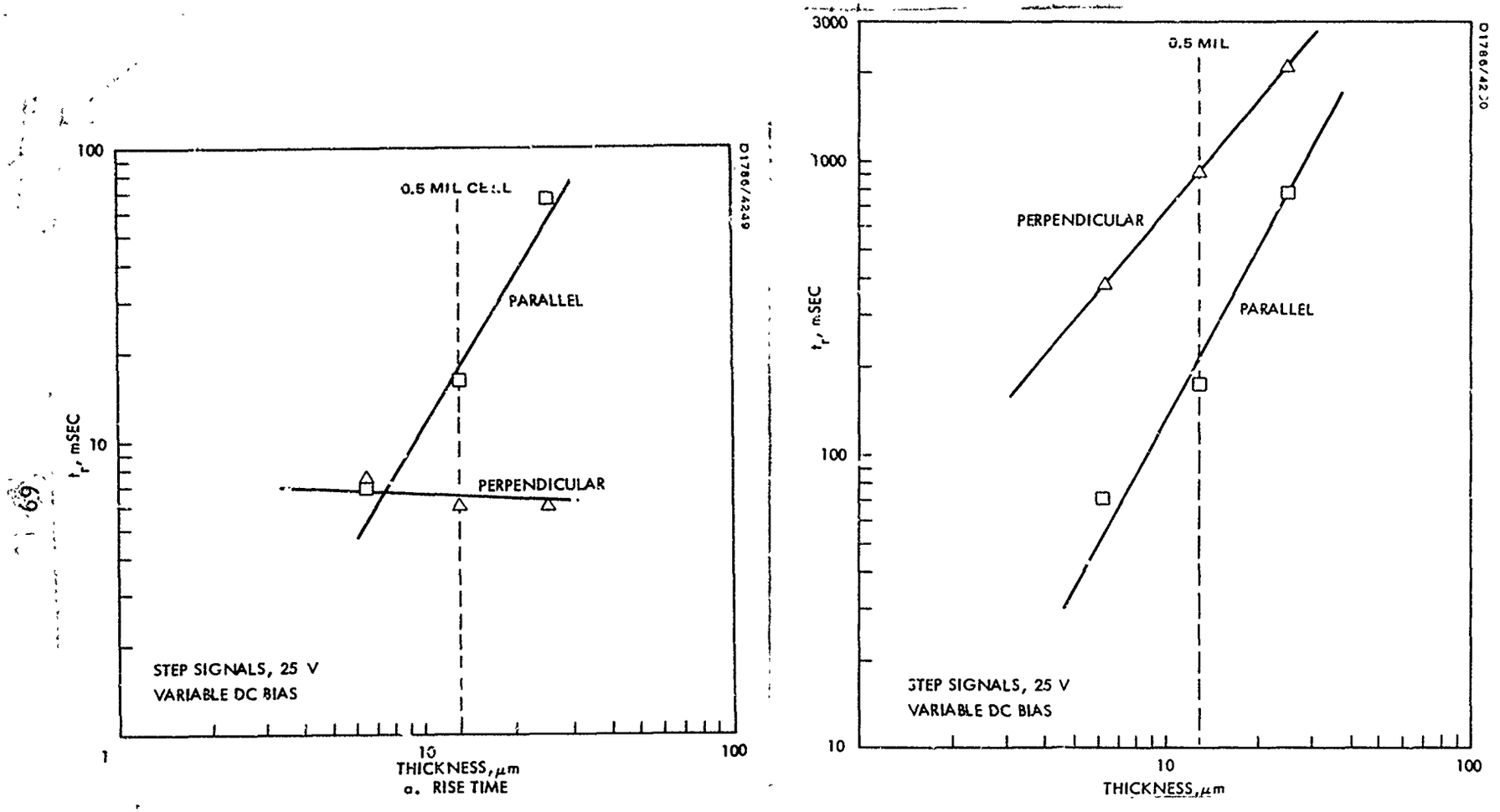
ϵ = dielectric Constant

E = electric field

This equation indicates that the speed of response is directly proportional to viscosity. For example, the sluggish response of LX materials at low temperatures is generally attributed to the increase in viscosity. However, data exist that indicate the converse may not be true because other parameters appear to be more influential at elevated temperatures. Fortunately, adequate speed of response can be obtained at room temperature and the display can be heated to maintain this speed during operation in cold environments.

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[3] Bonne, U. and Cummings, J. P., et al., Properties and Limitations of Liquid Crystals for Aircraft Displays, Honeywell Corporate Research Center, Final Report HR-72-285:4-35, October 1972, AD751667.



a. Rise time

b. Typical decay time

Figure 47. Effect of alignment orientation and thickness on speed of response.

Resistivity

The resistivity of the liquid crystal material influences the rise time of the scattering and the ultimate saturation scattering level. If the resistivity is too low, the elemental capacitor used for storage will discharge fully before the LX material has responded. If it is too high, there will be insufficient current in the LX material to generate the required scattering level. A computer simulation of LX material response indicates that the optimum resistivity occurs when:

$$RC/\tau \approx 2 \qquad \text{eq. 3}$$

where R is the resistance between the electrodes in an elemental cell filled with LX material, C is the capacitance of the elemental storage capacitor, and τ is the frame period. For the frame period and capacitance used in the LX airborne display, 1/30 sec and 10^{-11} farad respectively, the resistivity of the liquid crystal material should be approximately 2×10^9 ohm cm. With present synthesis techniques, the resistivity of the doped liquid crystal material prepared for use in the Liquid Crystal Pictorial Display typically ranges from 1×10^9 to 4×10^9 ohm cm. Resistivity values beyond 10^{10} ohm cm, as would be required in circuits having smaller storage capacitors and/or longer frame intervals are both difficult to formulate consistently and poorer in performance.

Alignment Dependence

The general shape of the electro-optic transfer curve is different when a perpendicular rather than a parallel alignment is imposed on the LX molecules. With perpendicular alignment, the curve has a sharp transition just above the threshold level and this makes it difficult to obtain the lower values of shades-of-gray as shown in Figure 48. Therefore, parallel alignment is the method now used for liquid crystal pictorial display.

ANTICIPATED PERFORMANCE

Present Characteristics

The 2N10 liquid crystal material has been formulated for laboratory use and room temperature display evaluation. It has a nematic range of approximately +14°C (57°F) to +54°C (129°F) and it is not a eutectic. For

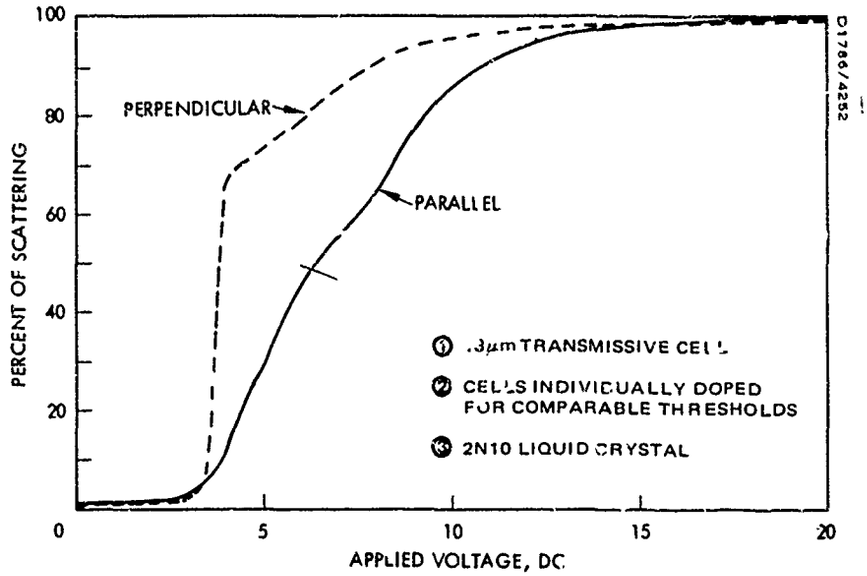


Figure 48. Effect of alignment on steady-state scattering.

the future, it will be necessary to formulate new mixtures similar to those suggested by Table 5. It has been estimated that the -54°C to +71°C range of MIL-E-5272C can be covered with a five component eutectic mixture.[3] The new material must have lifetime characteristics, scattering properties, speed and temperature range consonant with typical military requirements. In Table 6, objectives based upon typical military display indicators are stated, including the ability/status of the present technology to meet them.

For the Immediate Future

In HUD or in panel display configurations, the design approach will be to select an operating temperature for the display that is toward the upper end of the military indicator operating range and then tailor a liquid crystal (eutectic mixture) which will fall within the desired upper point. Heating will then be used to bring the display up to temperature and cooling will be used to bring the display from abnormally high temperatures (aircraft parked in sunlight, etc.) rapidly down to operating range.

Display Subsystem Heating

The amount of heating required is dependent upon the specific liquid crystal material formulation that is selected for use in the display. The

(3) Bonne, U. and Cummings, J. P., et al., Properties and Limitations of Liquid Crystals for Aircraft Displays, Honeywell Corporate Research Center, Final Report HR-72-285:4-35, October 1972, AD751667.

TABLE 6

TEMPERATURE RANGE OF THE LIQUID CRYSTAL PICTORIAL DISPLAY

REQUIREMENTS (TYPICAL MILITARY INDICATOR AMBIENT AIR ENVIRONMENT)	OBJECTIVES:	STATUS:
STORAGE – 62°C (–80°F) TO + 95°C (+203°F)	ELIMINATE DAMAGE FROM TEMPERATURE CYCLING OVER MIL SPEC RANGE	WORK UNDERWAY TO FORMULATE PRECISE EUTECTIC MIXTURES
ABNORMAL OPERATION – 54°C (–65.2°F) TO + 49°C (120.2°F)	EXTEND LOW-TEMPERATURE OPERATING RANGE BY HEATING THE DISPLAY.	THERMAL ANALYSIS COMPLETED; FEASIBILITY OF HEATING SHOWN.
NORMAL OPERATION – 18°C (–0.4°F) TO + 27°C (80.6°F)	OPERATE OVER RANGE TOLERATED BY HUMAN OPERATOR.	+ 14°C (57°F) TO + 40°C (104°F)

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plan at present is to select a material having the desired characteristics over a range of temperature near the maximum anticipated for the test aircraft. The display will then be heated to a temperature within that range; electrical resistance heating can easily be implemented, while cooling to a temperature below the inlet cooling air temperature is both complex and costly. The amount of power required to bring a HUD display of the type suggested in Figure 49 up to operating temperature from 0°C in one minute is estimated to be 100 watts based upon an assumption of 4 oz for the thermal mass of the display surface. The amount of power required to maintain the display at its operating temperature is comparatively small when reasonable amounts of thermal insulation are provided. If the heat radiated from the illumination source can be recovered economically, no additional power may be required to maintain the display at the operating temperature.

Display Subsystem Cooling

Cooling is required to rapidly bring the display down to operating temperature after it has been stored at an elevated ambient temperature such as in a closed cockpit on a sunlit runway. Several alternative methods have

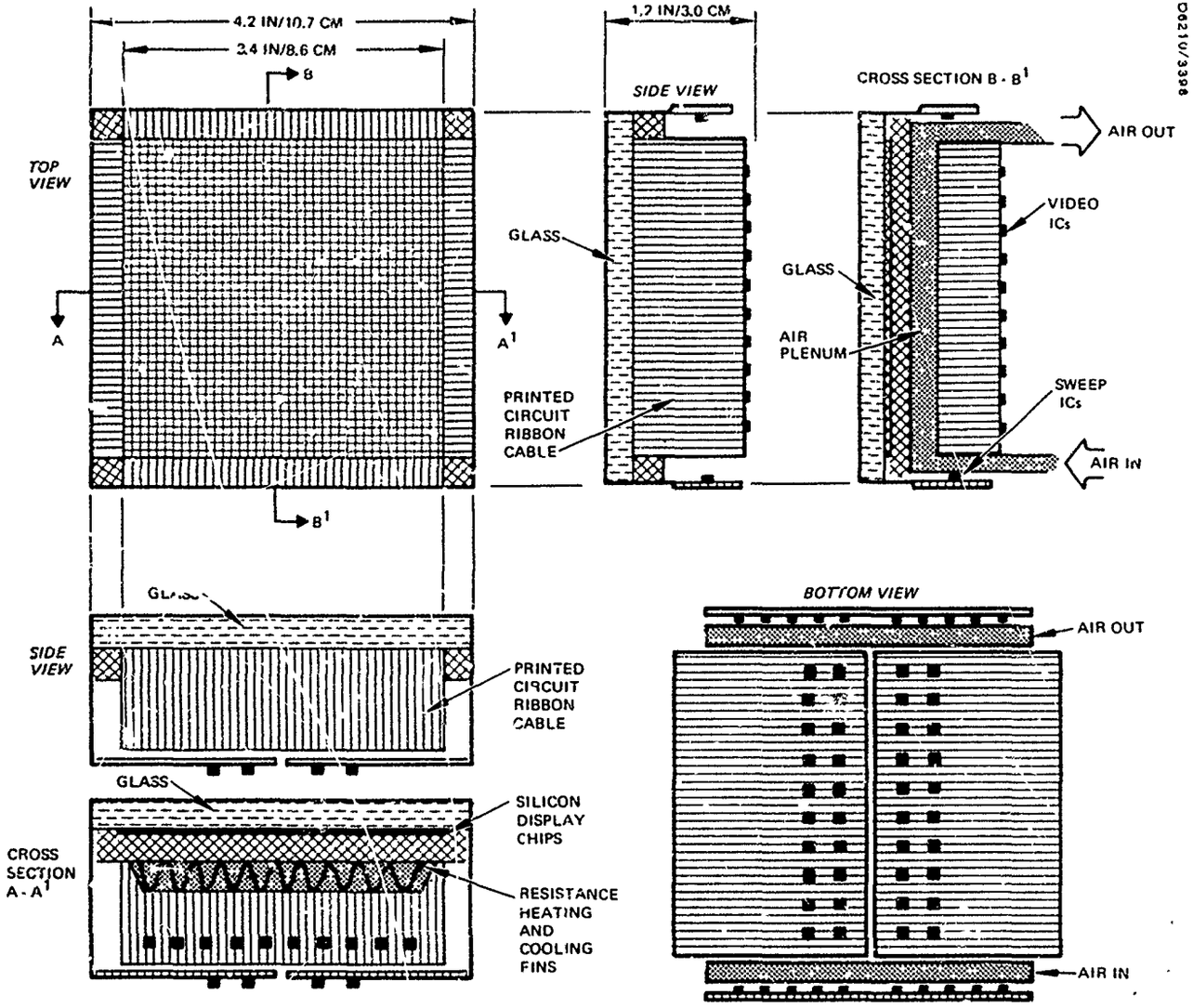


Figure 49. Suggested packaging arrangement for liquid crystal HUD.

been examined and their features are outlined in Table 7. Forced air cooling from the rear of the display as shown in Figure 48 (Remote Placement of Hybrid Packaged Custom LSI Chips) is believed to be the most logical approach. It can provide the required cooling at a minimum of additional cost and complexity.

TABLE 7

ALTERNATE DISPLAY COOLING APPROACHES

	Cooling Capacity	Temperature Controlability	Additional Volume and Weight	Additional Unit Cost
Convection and/or conduction from front panel	Very limited (Prevents rapid cooling of display)	None	None	None
Forced air cooling from rear	High (display can be rapidly cooled)	Fair (electro-mechanical thermostatic)	Moderate	Small
Peltier cooling	Moderate	Excellent (electronic)	Moderate (requires additional conventional cooling)	Moderate
Forced fluid cooling	Very high	Good	Small but heavy	Moderate to high

SECTION IV

ILLUMINATION AND VIEWING

The illumination of liquid crystal display devices is inherently efficient because of their low optical absorption coefficient. A reflective display mode is normally employed, and so virtually all of the incident light is retransmitted, with only a small amount absorbed at the reflecting surface. The display is essentially passive since its operation results in the modulation of available light rather than the generation of "new" light. However, the characteristics of the image presented are largely determined by the optical characteristics of the liquid crystal material being used. Therefore, requirements for the illumination and viewing system of a liquid crystal display must first be examined in terms of the liquid crystal material being used. There are two types commonly used for displays: field effect and dynamic scattering.

Field-effect materials, to be useful, normally require two polarizing filters. There is an inherent light loss of over 50 percent due to these filters alone, and so the power requirements of the lighting system are greatly increased. In Head-up Display applications it is necessary to have an extremely bright display to maintain contrast against the high ambient lighting conditions, so the use of field effect materials is considered undesirable in terms of the power required. In panel display applications, polarizers limit the viewing angle to an unacceptably small area. Furthermore, the second polarizer required on the reflective electrode array surface cannot be provided at the present time. For these reasons a dynamic scattering mode of operation has been chosen for the liquid crystal airborne display.

The dynamic scattering mode of operation, while offering possibilities for increasing the efficiency of luminous displays to a degree not possible in earlier conventional displays, places unique requirements on the design of illumination and viewing systems. Theoretically, 100 percent contrast could be achieved with the technique. However, the practical limits on contrast, as

well as on the luminous efficiency of the display, depends upon the degree to which the illumination-viewing system separates specularly reflected rays away from the viewer, while directing diffusely reflected (scattered) rays toward him.

Lighting methods were categorized into those that apply chiefly to directly-viewed panel displays and those that are more applicable to magnified or indirectly viewed displays such as a HUD.

The techniques that are discussed in the section that immediately follows are chiefly of interest for panel display applications, although night-illumination and circular polerization techniques are somewhat applicable to both directly-viewed and to magnified-displays. A separate section (Head-Up Displays) will deal with schlieren techniques and illumination methods that are of interest for both conventional-optics HUDs and advanced designs using hologram optical elements.

PANEL DISPLAYS - SUMMARY OF LIGHTING METHODS

The lighting methods examined for panel display applications are discussed in this section. Each is essentially a means for separating diffuse from specular light. As it happens, each method utilizes the scattered component as the positive image, although systems such as light valves have been designed where operation using scattering to reduce the light intensity is used to advantage. The techniques to be discussed are:

- Offset luminaires and light trap
- Wedge light guide
- Circular polarization of ambient light
- Skylight

Offset Luminaires and Light Trap

By far the most common means of utilizing a reflective liquid crystal display is to illuminate it from an angle which makes the diffusely reflected image visible to the observer, while deflecting the specular image of the light source out of the field of view. Similarly, the viewing angle with respect to the display plane is deliberately arranged to insure that all objects

normally seen by specular reflection are of very low luminance; this is accomplished by taking advantage of a dark area such as the floor of a room or by installing a "light trap".

The scattering effect of the liquid crystal surface is not lambertian. This means that light is not reflected from the display surface uniformly in all directions for a given incident ray. The reflection characteristic, when under excitation, is more like that of a motion picture screen, with a somewhat stronger component along an axis coincident with the specular reflective axis, and weaker reflectance as the angle away from this axis increases. This means that the closer to the specular angle the display can be viewed, the greater the intensity of the reflected light. This principle has been observed in the designs described below, which always provide for exclusion of the direct specular beam from the eye. For mathematical simplicity in certain of the analyses, lambertian scattering has been assumed. This approximation has been made only where it does not affect the conclusions drawn from the analysis.

The sketch of Figure 50 shows the basic principle of offset illumination. Scattered light from the excited display surface reaches the observer's eye

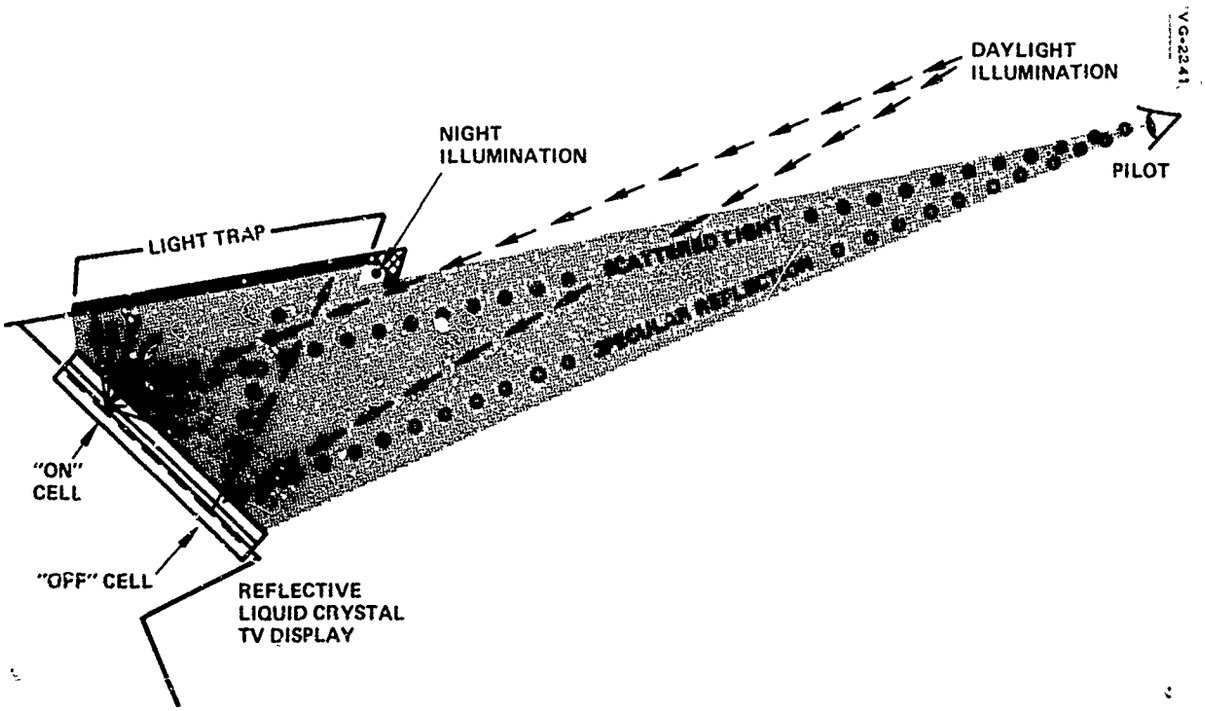


Figure 50. Liquid crystal display operation.

at an angle slightly greater than the angle of specular reflectance, whereas the sources which may be viewed by direct specular reflectance are either blocked or effectively absorbed by a "light trap". The photograph (Figure 51) illustrates the scheme mocl d up to mount in front of an optical sight in a single-place aircraft cockpit.

Figure 51. Flat panel liquid crystal display added to front face of optical sight mechanism in single place F-4 aircraft installation.

Wedge Light Guide

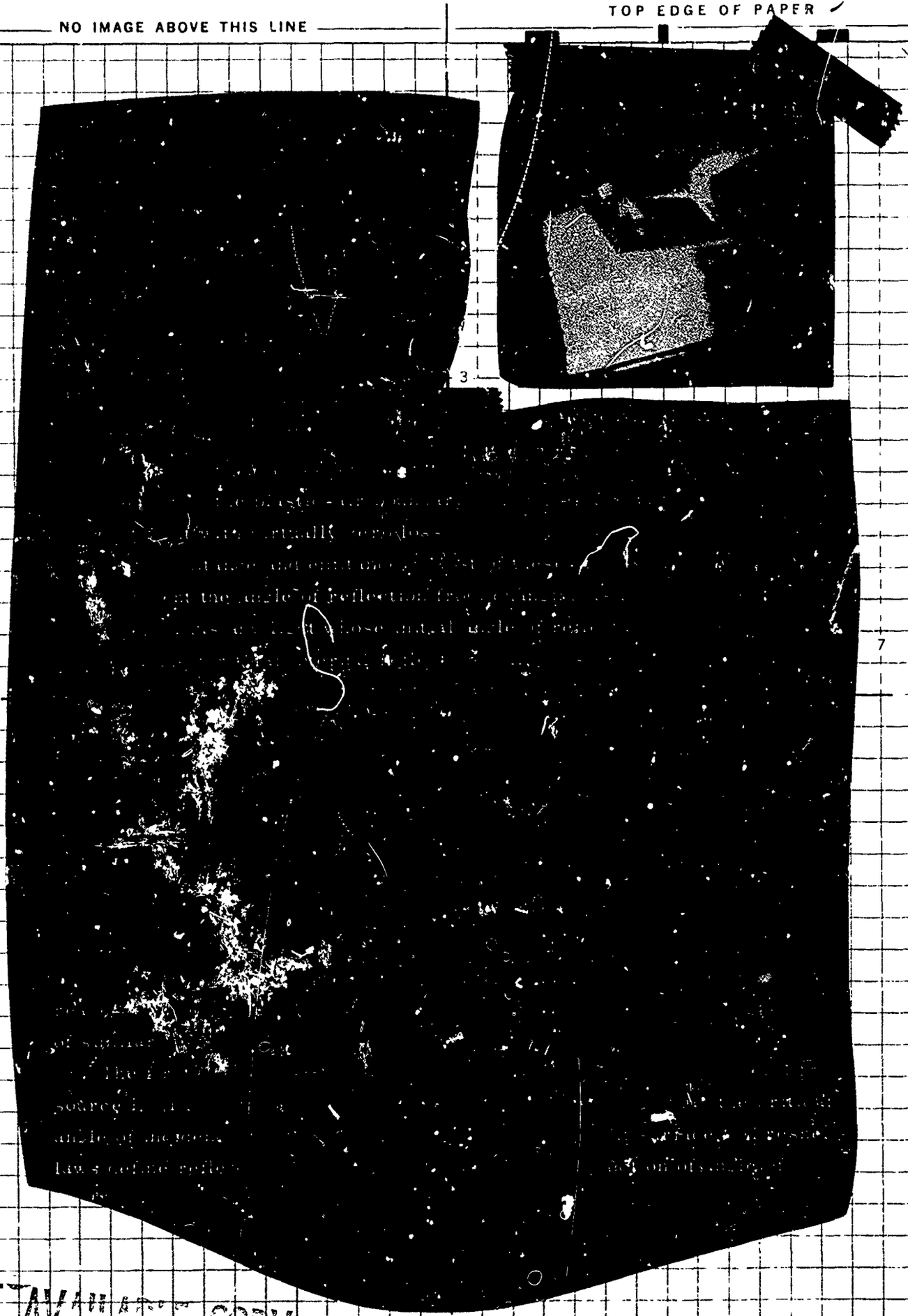
Plastic light guides depend on internal reflection from the plastic-air boundary to direct light with virtually zero loss except at immitance and emitance. Most of these utilize parallel surfaces, which prevent the angle of reflection from changing as light travels down the guide. Thus any light whose initial angle of reflectance exceeds the critical angle for total internal reflection will, on subsequent reflections, maintain the same angle as that of the first reflection and continue downstream until it meets the end of the tube or other intended alteration in surface shape. Fiber optics, and edge lighting of engraved legends, are examples of this type of design.

Consider the case in which the surfaces of the plastic are not parallel, but converge away from the light source. Figure 52 shows such a "wedge", of angle b, and height H, the latter being measured from the illumination source I to the apex 0 of the wedge. The several design characteristics of the wedge light guide are evident in the figure. For simplicity, these will be developed intuitively from the drawing; the reader will note that they can easily be proven geometrically by means of similar triangles.

The first bracket set of small arrows labelled "1" represents light from source I. This light, which strikes the top surface at less than the critical angle of incidence c, is mostly transmitted through that surface. (Fresnel's laws define reflection at a dielectric boundary as a function of angle of

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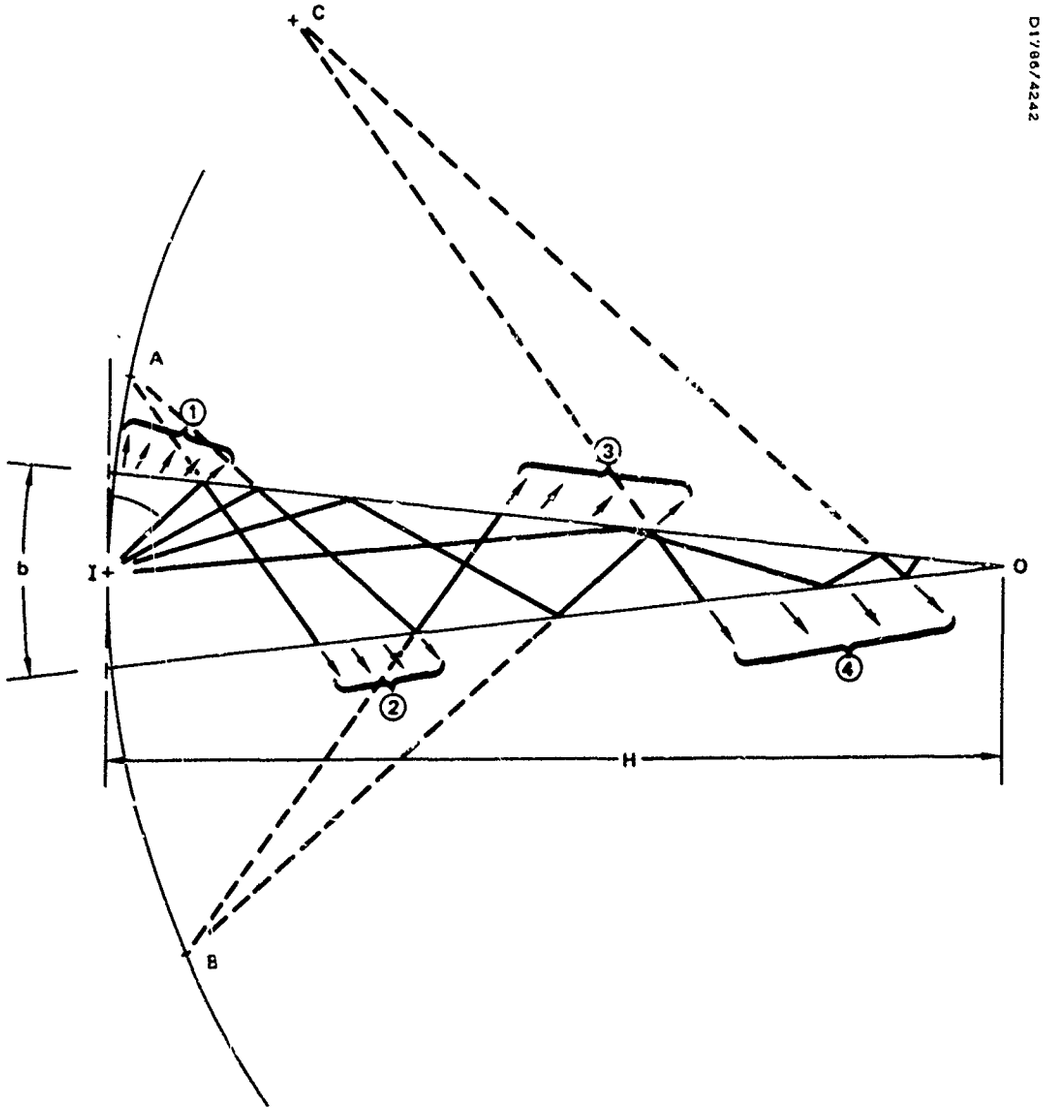


Figure 52. Schematic of wedge light guide. Bracketed arrows are bands of illumination.

incidence for both vectors. In the present discussion, a simplifying assumption is made, namely that light is wholly transmitted at angles of incidence less than the critical angle, and wholly reflected at angles greater than the critical angle. Actually a minimum of 4 percent of the incident light is reflected at any angle, and polarization occurs. It is greatest at the Brewster angle of about 62 degrees for methacrylate resins like Lucite and Plexiglass [neither of these effects is significant in the present context].

Beginning at 12 o'clock and proceeding clockwise around Source I, we reach a point at which the angle of incidence on the top surface is equal to the

critical angle, c. This is the limit at which light is transmitted within the bundle labelled "1"; all further rays will be reflected toward the bottom surface. The conjugate point for these reflected rays is indicated by the letter "A" in the diagram. Because of symmetry about the top surface, it will be noted that Conjugate Point A and Source I are equidistant from the apex of the wedge, 0.

Continuing in the clockwise direction, because of the angle of the wedge, the first ray to be reflected from the top at the critical angle strikes the bottom at b degrees (the wedge angle) less than the critical angle and is consequently transmitted through the bottom surface. Subsequent rays will be similarly transmitted until the critical angle is again reached. At this point rays striking at greater angles will be reflected upward to the top surface. The angle subtended by the ray bundle transmitted through the bottom, indicated by the bracketed set of small arrows labelled "2", is thus exactly equal to the wedge angle, b.

By similar reasoning another ray bundle, which subtends the same angle, is transmitted through the top surface, labelled "3". The conjugate point for this bundle is B. By symmetry with the bottom surface, B and A are seen to be equidistant from the apex; B and I are thus also equidistant. In fact, the locus of <u>all</u> of the conjugate points is a circle of radius equal to the height, H, of the wedge.

Because A and I are equidistant from the top surface, and a line drawn from I to 0 (not shown) bisects the angle of the wedge, it follows that the angle AOI is equal to the wedge angle. Similarly COA and IOB are equal to twice the wedge angle, and so forth.

The process can be continued until all of the light emanating from I into the wedge is accounted for. The drawing could be turned over to show that the rays remaining toward the bottom will emerge in similar bands falling exactly between those already drawn, with their conjugate points exactly between those already located on the circle. Because the bands in the figure are smaller than the spaces between them, it is also clear that the complementary set of ray bundles will not fill in the spaces, but will always leave some dark surface area in between; this is true regardless of the angle of the wedge.

Light leaving the wedge is not transmitted in the direction shown in the figure, but is deflected at the plastic-air boundary. Figure 53 shows the

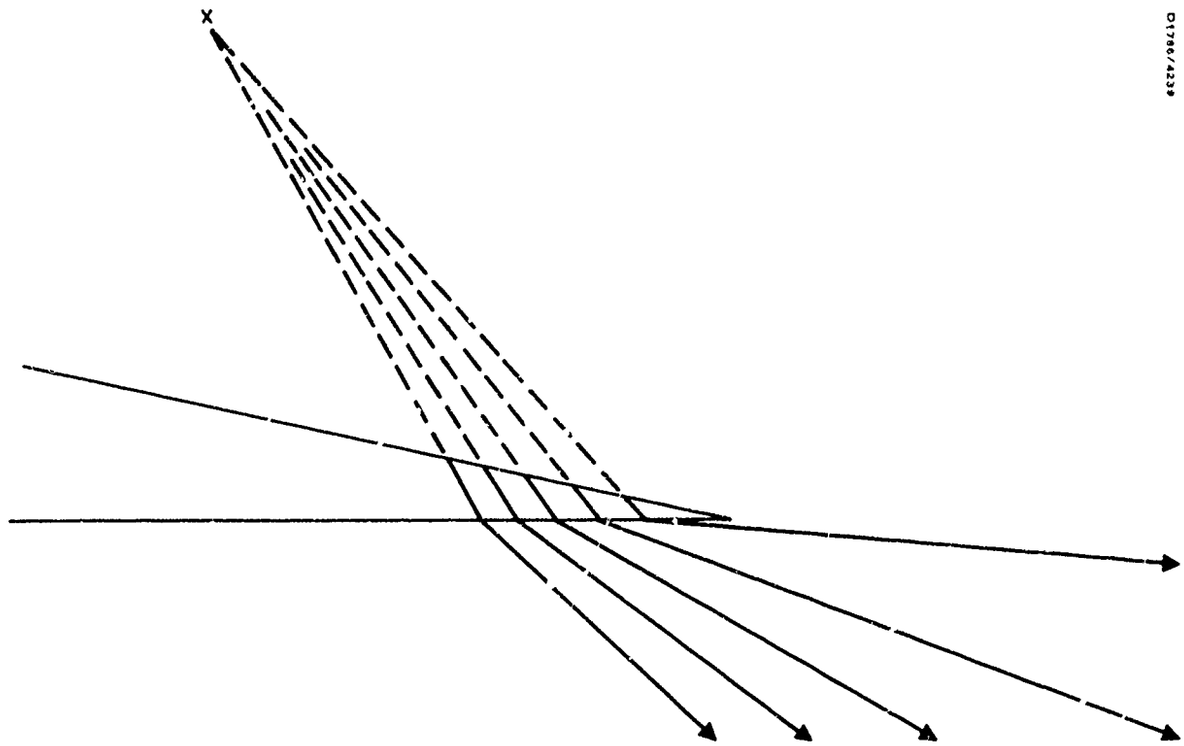


Figure 53. Emergence pattern of band as it traverses wedge-air boundary. Refraction at boundary bends light toward apex of wedge.

emergence pattern for rays in a typical emittance band. This dispersive characteristic tends to produce very uniform illumination at short distances from the wedge, even though relatively few bands are present. It will be shown that the number of bands is related to the angle of the wedge, becoming greater as the wedge angle is decreased.

The foregoing provides some insight into the geometrical optics of wedge light guides, and illustrates two significant advantages of the devices when used for the illumination of liquid crystal surfaces: they provide a truly diffuse light source at a nearly optimum angle of incidence to the display, and they require very little additional volume behind the panel because all light distribution takes place within the display "window" itself. We shall now show a simple construction for a design of wedge light guides, and then develop some optimization tradeoffs.

Figures 54 through 56 show the geometrical derivation of the emittance characteristics of a 5-inch 12-degree wedge fabricated from Plexiglass, whose refractive index of 1.49 yields a critical angle of 42.16 degrees.

Recalling that all of the conjugate points fall on a circle whose radius is equal to the distance of the light source from the wedge apex, and whose center is at the apex, the first step is to lay out such a circle against the outline of the wedge. Conjugate points can then be located by marking every 12 degrees (the angle of the wedge) along the circle in both directions from

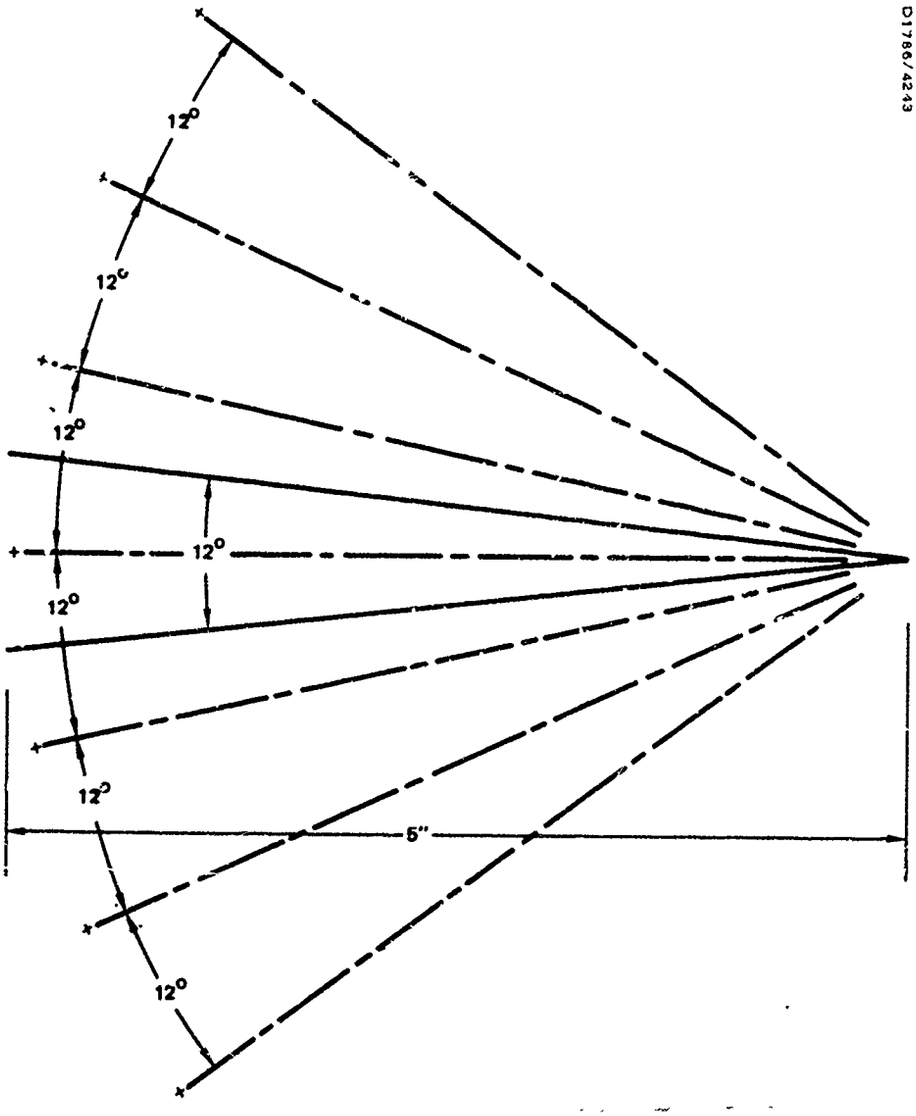


Figure 54. First step in geometric construction of wedge.

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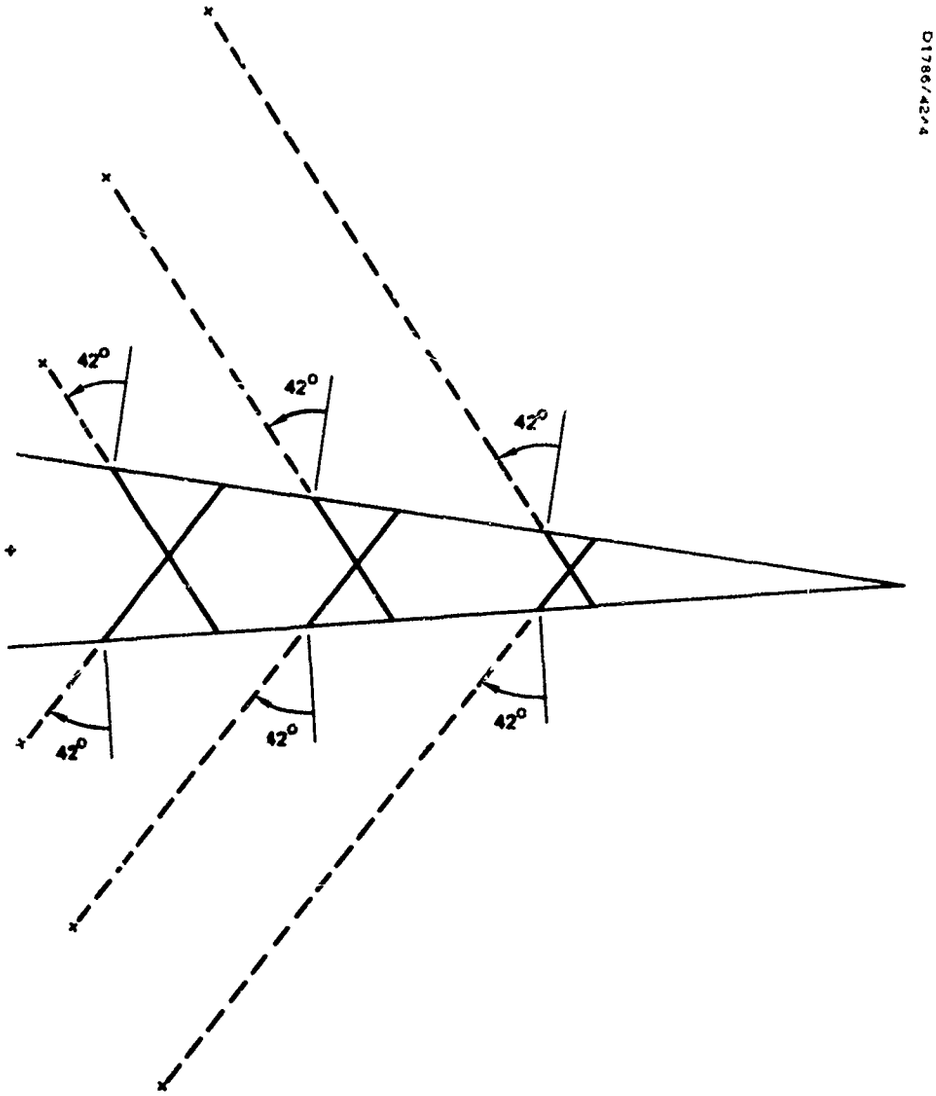


Figure 55. Second step in construction of wedge design.

the illumination source, staying within the critical angle of 42 degrees (Figure 53).

Parallel lines can now be drawn between the bottom surface and the top, crossing the top surface at the critical angle of incidence, 42 degrees, as shown in Figure 55. Lines are also drawn upward from the lower conjugate points crossing the bottom surface at the critical angle and terminating at the top surface.

The outlines of the ray bundles are completed by drawing a second line from each conjugate point at an angle to the first exactly equal to the wedge

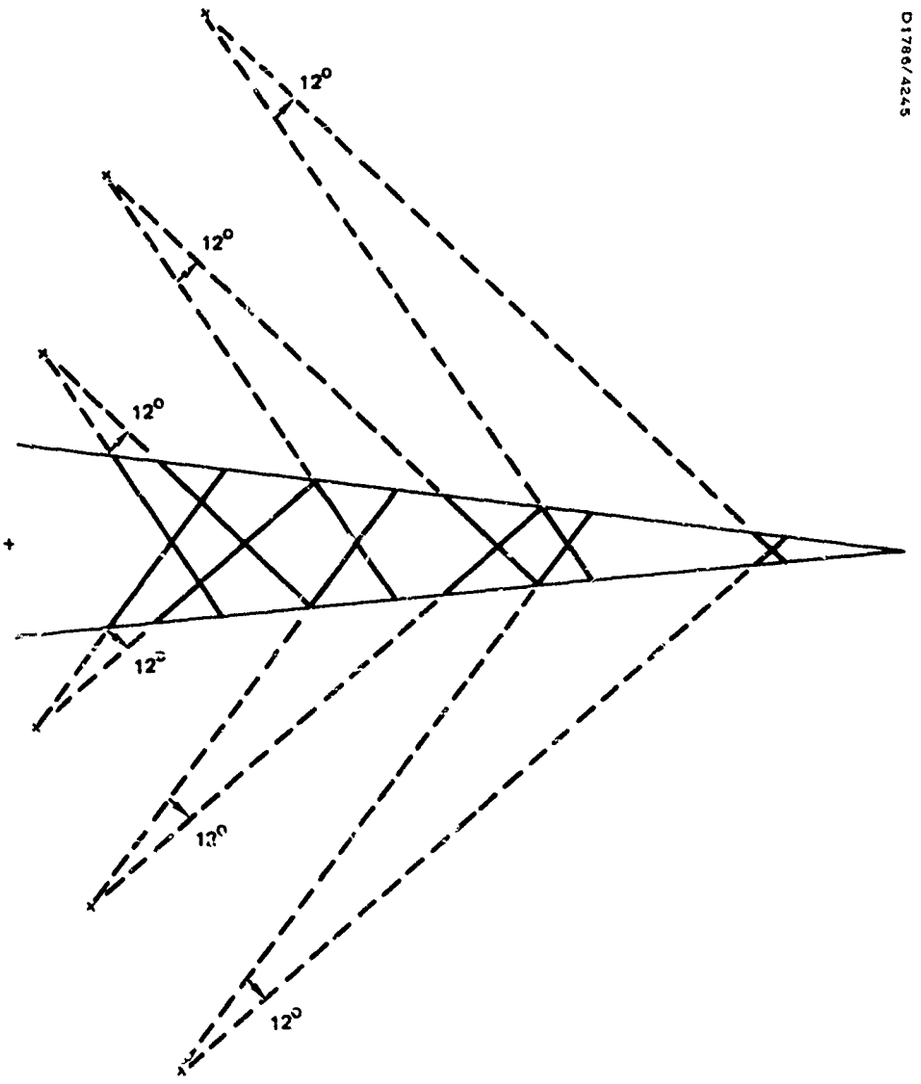


Figure 56. Third step in wedge construction.

angle, 12 degrees. This second line is drawn at an angle toward the apex, as shown in Figure 56. The intersection of each ray fan with its opposite surface is an emittance band for that surface. If the designer is interested only in the emittance radiating from one side of the wedge, only half the construction need be made.

Finally, the minimum angle of emittance is related to the angle of incidence by the equation

$$e = \arcsin [n \sin(c - b)] = \arcsin [1.49 \sin(42 - 12)] = 48 \text{ degrees}^{*} \quad \text{eq. 4}$$

where

e = angle of emittance
n = index of refraction
c = critical angle
b = wedge angle.

Figure 57 shows these limiting rays added to the diagram.

A 12-degree wedge was used as an example because the relatively small number of bands permitted a simple drawing. It is not a practical example for a number of reasons. In the first place, the resulting illumination would not be especially uniform; also the number of bands is small. Such a thick wedge (12°) would require an inordinate amount of material for even a small display surface. About one fourth of the linear dimension of the wedge is wasted because of the extreme width of the bands. And finally, viewing a display surface through such a thick wedge (essentially a prism) would result in chromatic fringes and the apparent tilting away of the surface from the observer. We shall now consider means of optimizing the design of wedge light guides.

Two things happen as the wedge angle is decreased. Closer spacing of the conjugate points along the circle increases the number of emittance bands for a given wedge length, and reduces the "inactive" surface adjacent to the illumination source; also the emittance angle increases, so that emerging rays will strike a parallel display surface at more and more of a grazing incidence. In the limit, the wedge becomes a parallel light guide.

The number of bands is equal to the critical angle divided by the angle of the wedge. Additional insight into the uniformity to be anticipated with a given design may be obtained by computing the width of the first few bands from the following equation:

$$W_n = H \operatorname{cct} c \{\cos [c + (n-1)b] - \cos (c + nb)\}^{**} \quad \text{eq. 5}$$

*From Snell's Law: $n_1 \sin \omega_1 = n_2 \sin \omega_2$

**Developed by the method of similar triangles from the schematic of Figure 61.

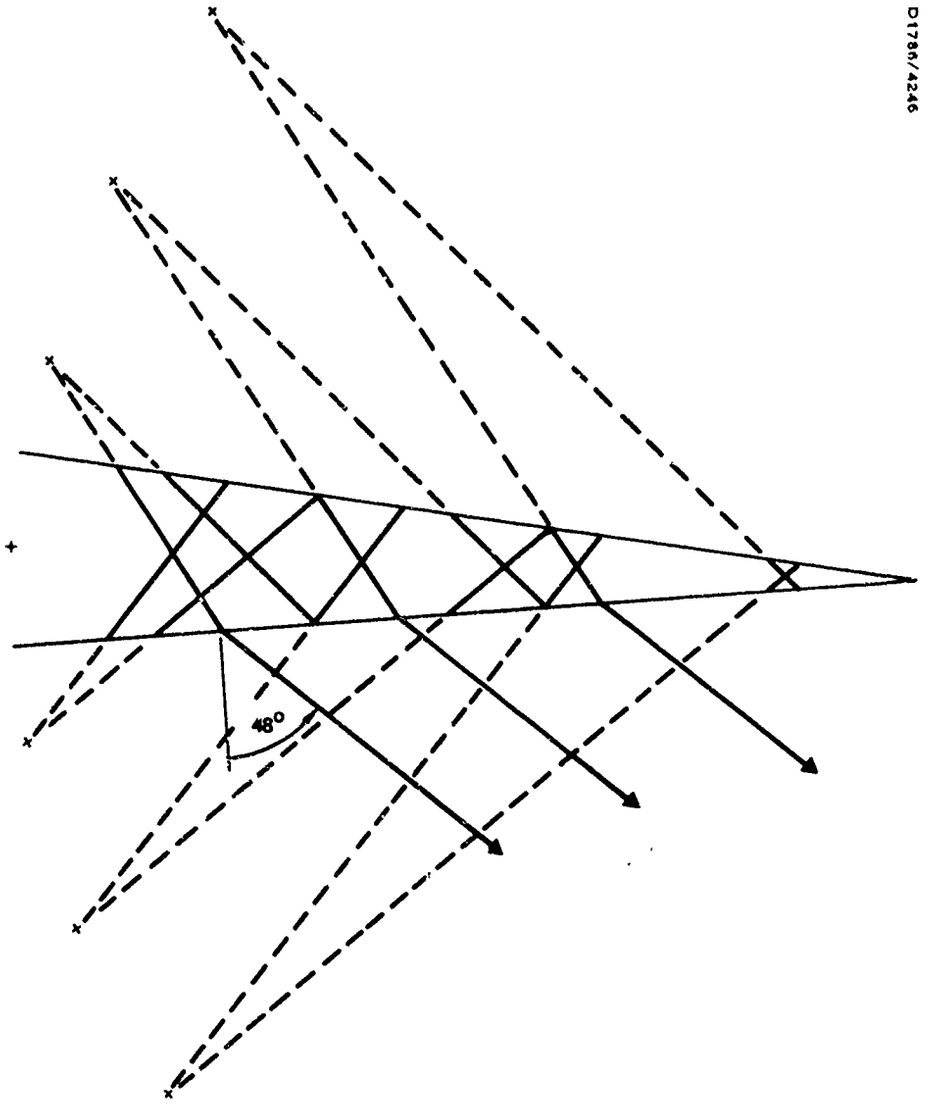


Figure 57. Plotting emergence angles for wedge.

where

H = radius wedge, apex to illuminated edge

W_n = width of nth band

c = critical angle

b = wedge angle.

The width of the first band is plotted as a function of wedge angle for a 3-inch wedge in Figure 58. If one makes the reasonable assumption that the

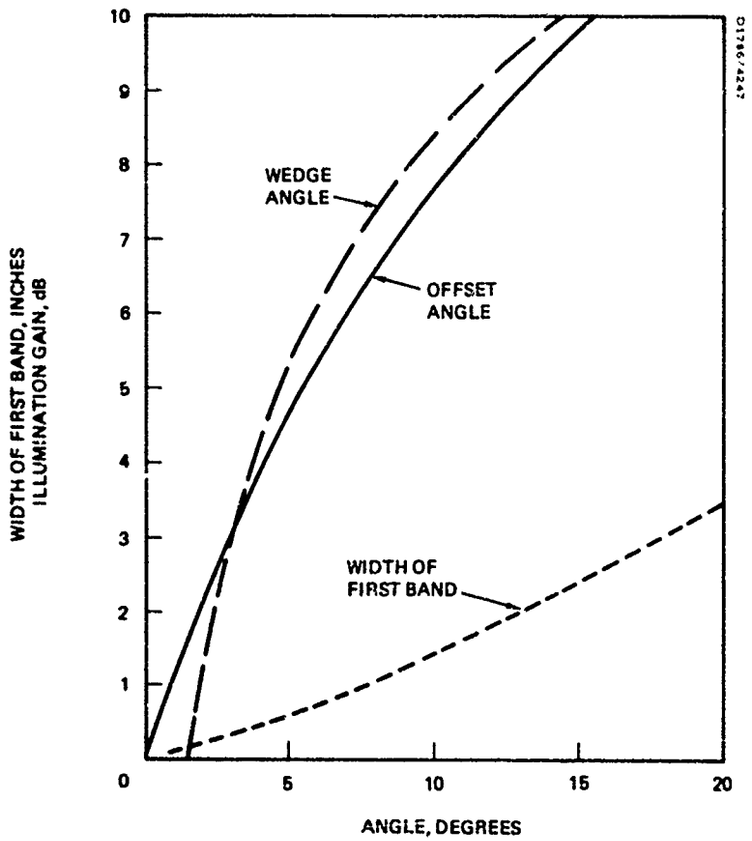


Figure 58. Illumination efficiency and width of first band as function of wedge angle and angle of offset.

first band should not be wider than the wedge-display separation, then the wedge angle must be less than 5 degrees for separations of one half inch or so. A 5-degree wedge would yield 42/5 = 8 bands in all, which also augurs well for acceptable uniformity.

The effect of increasing the emittance angle with decreased wedge angle is to reduce the efficiency of the illumination due to the grazing incidence of the light on the display surface. The average reflectance over the angle β of the ray fan is equal to

$$\overline{R} = \int_0^{\pi/2} \cos\beta \, d\beta = \frac{1 - \sin\beta}{\frac{\pi}{2} - \beta}^{*} \qquad \text{eq. 6}$$

(Two simplying assumptions are made. Flux density within the ray fan is assumed to be constant as a function of angle; and Lambertian reflectance is assumed.)

*Standard expression for lambertian reflectance.

Figure 58 also shows the effect of angle of incidence on illumination efficiency as a function of wedge angle. Here a 1.5-degree wedge is taken as a practical minimum, and the gain in efficiency is given in decibels over that which would be obtained with the 1.5-degree device. If uniformity were not important, it is obvious that considerable advantage could be gained by increasing the wedge angle as much as display visibility would permit. (Recall that thick wedges are accompanied by chromatic aberration and display tilting.) Table 8 presents representative calculations as a function of wedge angle, b, of emittance angle, average reflectance, $\overline{R}$, decibles gain over a 1.5-degree wedge, and the width of the first band.

One further step may be taken toward increasing reflective efficiency. The incident angle of the emitted light against the display surface may be increased by tilting the wedge slightly away from the surface. There are severe limitations to this, because the top surface of the wedge and the display surface, since both are reflective, tend to direct reflections of light source into the observer's eye at relatively small angles of tilt; however it is a practical technique over 5 to 10 degrees when the display is to be viewed at normal cockpit distances. The effect of tilting the wedge light guide through a given offset angle with respect to the display surface comprises the third and final curve of Figure 58. This is also rendered in decibels, this time with respect to zero offset angle.

TABLE 8

CALCULATED PARAMETERS FOR REPRESENTATIVE WEDGE ANGLES

Wedge Angle, b	Minimum Emittance Angle, deg	Average Reflectance	Gain, dB	Width First Band, in
1.5	13.86	0.120	0	0.22
2.0	16.05	0.139	1.3	0.29
2.5	18.00	0.156	2.2	0.36
3.0	19.78	0.171	3.0	0.44
4.0	22.97	0.198	4.3	0.59
5.0	25.82	0.222	5.3	0.74
7.0	30.88	0.263	6.8	1.06
10.0	37.50	0.316	8.4	1.55
15.0 deg	47.12	0.389	10.2	2.41

Design optimization, then, consists of selecting the greatest wedge angle and display offset angle consistent with uniformity, in the first case, and viewing angle, in the second. If the display is to be viewed over a wide range of angles, probably no offset whatsoever should be employed, and the wedge should have an angle of 2 to 3 degrees, both at some cost in efficiency. If the viewing angle is restricted, as in a cockpit, both can be increased. In no event does it appear that angles greater than 5 degrees will be useful in a practical display, although larger angles would increase illumination efficiency. The foregoing will provide guidance in arriving at a design. Figure 59 shows a construction for a 5-inch, 3-degree wedge which was mocked up in the Hughes laboratory for use with a fluorescent light source. A 3-inch (useful area) 5-degree wedge, mounted at 5 degrees offset for maximum efficiency with a low level tungsten source, is shown in Figure 60.

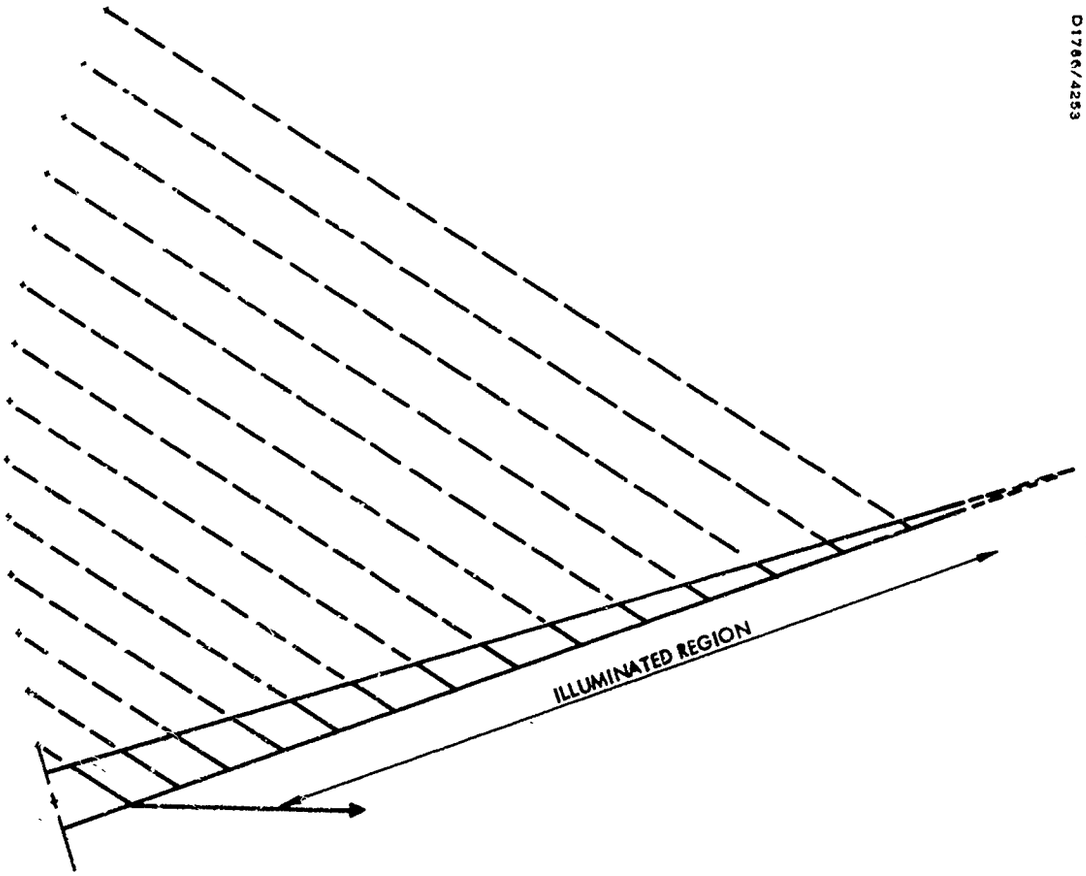
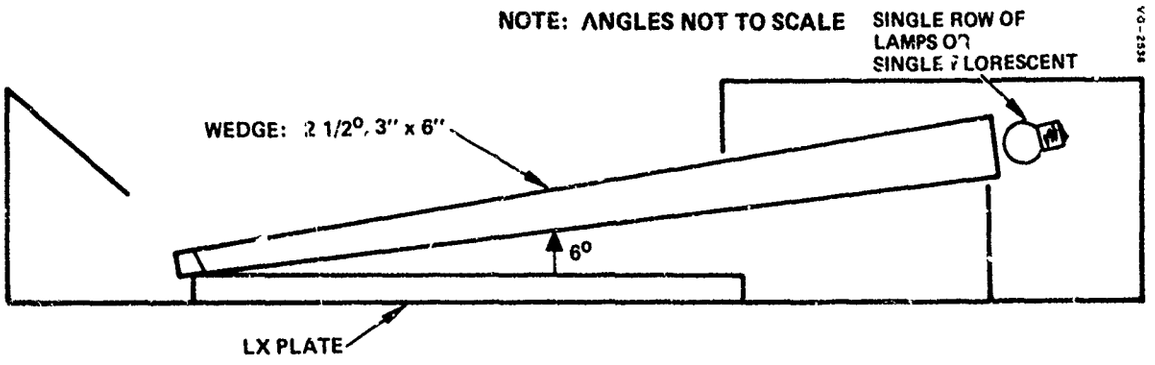


Figure 59. Geometric construction for five-inch, three-degree wedge.



a. characteristic geometry

b. photograph of unit in operation

Figure 60. Wedge lighting mockup.

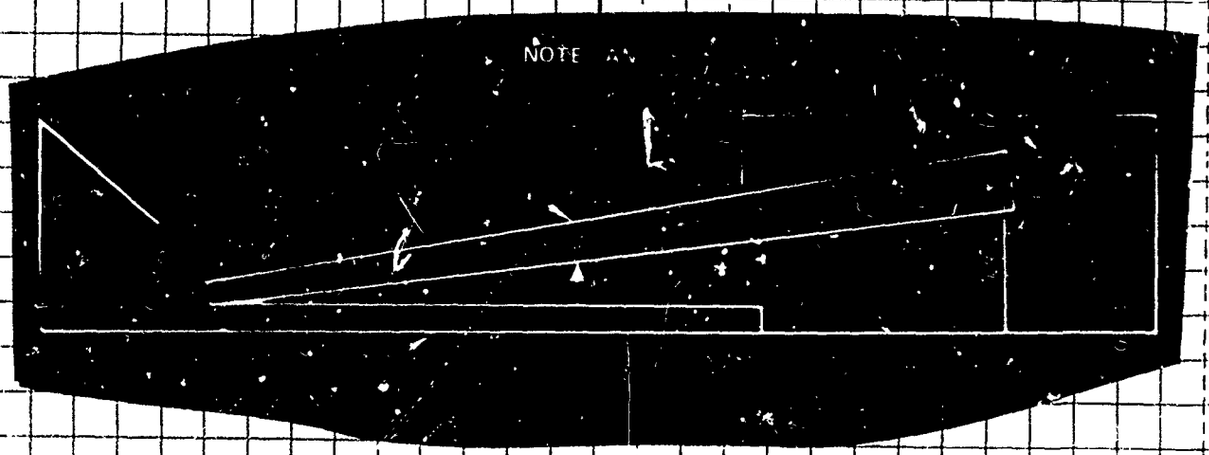
Circular Polarization of Ambient Light

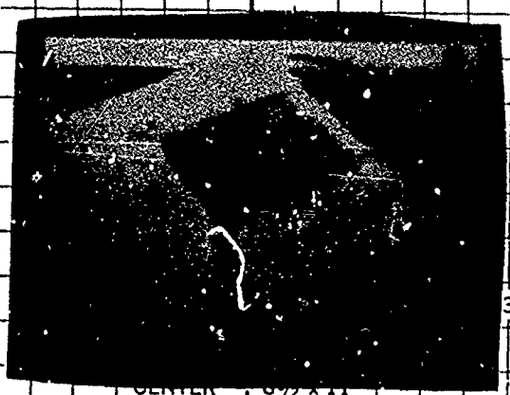
Circular polarization is another way of separating diffuse from specular light. The concept is intuitively appealing for reflective liquid crystal devices, due to the high absorption exhibited by most circular polarizers under specular reflection. It is not practical for a reflective liquid crystal surface, however.

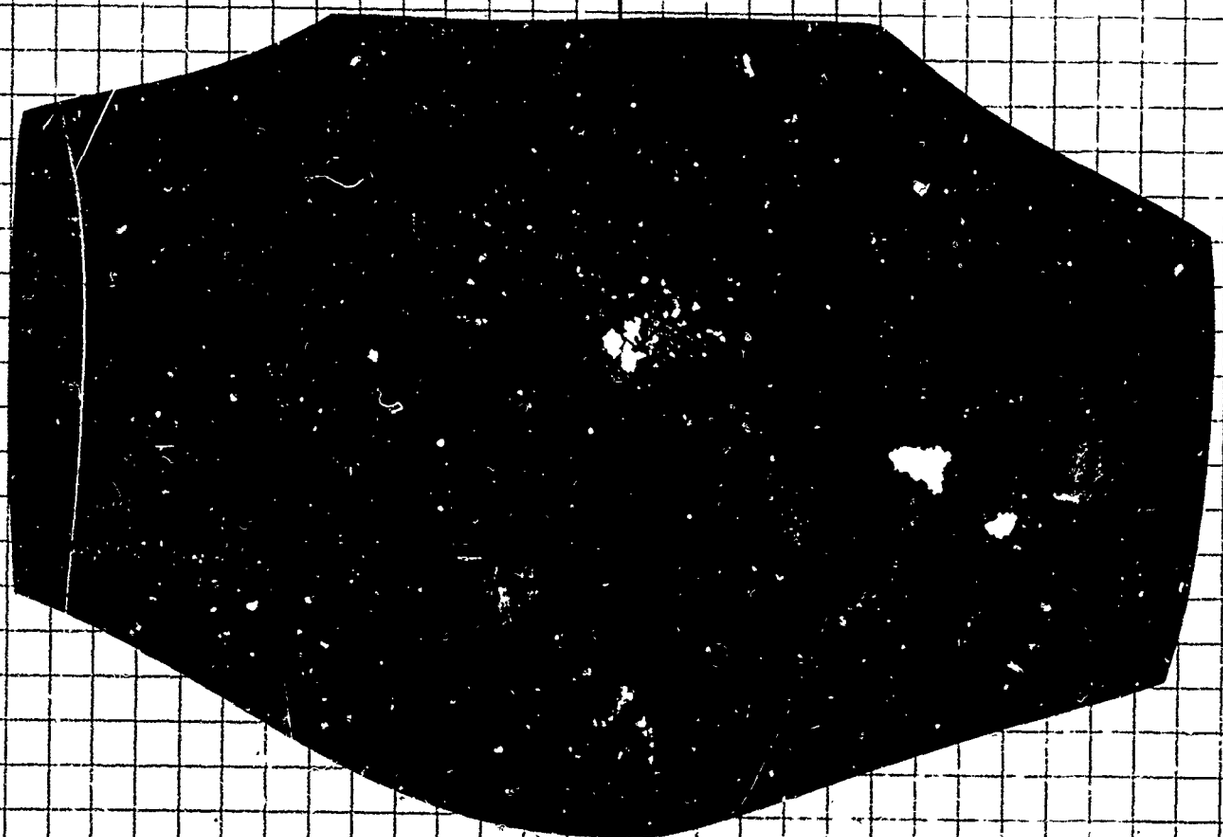
Figure 61 shows the customary "circular polarizer", which comprises a sheet of linear polarizing material cemented to a quarter-wave retardation plate. Incident light, plane-polarized as it passes the first time through the

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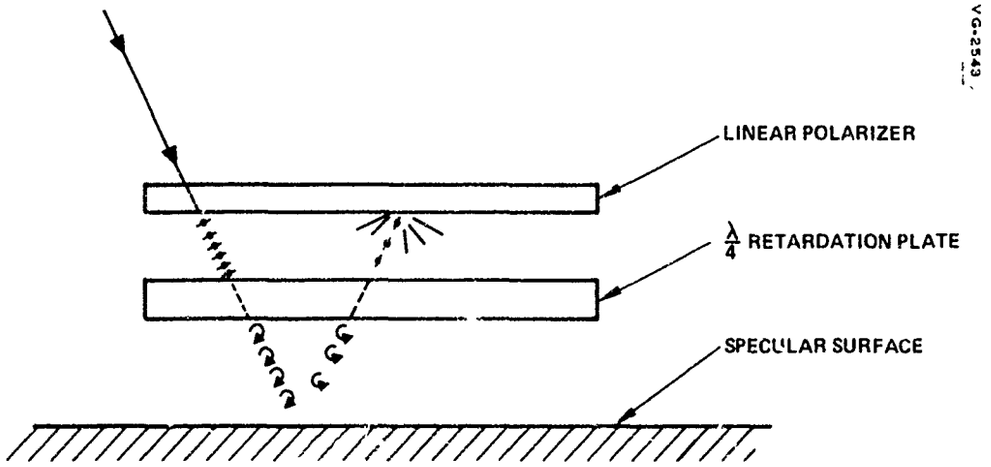


Figure 61. Design configuration of a circular polarizer.

polarizing material, is retarded in phase in one vector by a quarter wave as it traverses the birefringent quarter-wave plate. The direction of rotation is changed by the 180-degree phase reversal occurring with specular reflection. On the second passage through the quarter-wave plate, then, the 90-degree retardation reconstitutes the beam into linearly polarized light, which is now crossed with respect to the original plane of polarization and hence is absorbed by the linear polarizer. Scattered light, on the other hand, the phase of which is randomized by the scattering, passes through the linear polarizer with only the normal attenuation of the dyes.

The rejection of specularly reflected light by a circular polarizer is thus dependent on the capacity of the birefringent material to retard phase exactly 90 degrees. But nematic liquid crystals, like nearly all optically active materials, are also birefringent. Consequently the phase shift resulting from the birefringency of the liquid crystal is added to that occurring in the quarter-wave plate. Worse, the high degree of birefringency results in delays of many wavelengths, such that control to the accuracy required of a quarter-wave plate is virtually impossible.

Separation of specularly reflected light from diffusely reflected light by simply placing a circular polarizer over the liquid crystal surface is therefore not presently a practical solution. A better solution would be to insert the circular polarizer between the liquid crystal and the specular reflector. Although this technique is feasible for simpler displays: alphanumerics,

wrist watches, and etc., it is not compatible with the present technology and the materials used for the construction of the semiconductor matrix of the liquid crystal display.

Skylight

Most practical installations for a liquid crystal display place the display surface in such a way that direct reflection of either sun or skylight into the pilot's eyes is precluded. A distinct advantage of the liquid crystal technique, however, is that any light source, including ambient, can be used. While a number of implementations combining ambient with artificial light can be imagined, it is useful to consider a worst case, in which light reaches the display surface through a window of restricted dimensions, while the pilot and the cockpit are illuminated by direct sunlight. The light source for the display, under these conditions, is the sky itself, inasmuch as the possibility of the sun being at exactly the proper position over any extended period of time is small.

Light falling on a surface from a diffuse source like the sky through a square window of S units along a side, located D units distant from the surface, is related to light falling through a window of infinite extent by the following equation:

$$\text{Light} = \frac{\text{Light through small window}}{\text{Light through infinite window}} = \frac{4S \text{ ARCSIN}\left(\frac{S}{\sqrt{2S^2 + 4D^2}}\right)}{\sqrt{S^2 + 4D^2}} \quad \text{eq. 7}$$

Figure 62 shows a plot of this function for windows as large as 24 inches on a side, located at distances of up to 20 inches from the display surface. The dashed line represents what appears to be a practical limit of a window whose dimensions are the same as the distance from the surface. Larger ones are possible, of course; but it is likely in a practical installation that a window of this size or smaller would be employed. The attenuation, or system gain, under this condition is 0.24.

The Handbook of the Illuminating Engineering Society lists skylight values for various latitudes in the Northern Hemisphere. These range from 750 to 2,700 footlamberts at noon, depending on latitude and direction; illumination from the sun follows a similar pattern. The lowest display

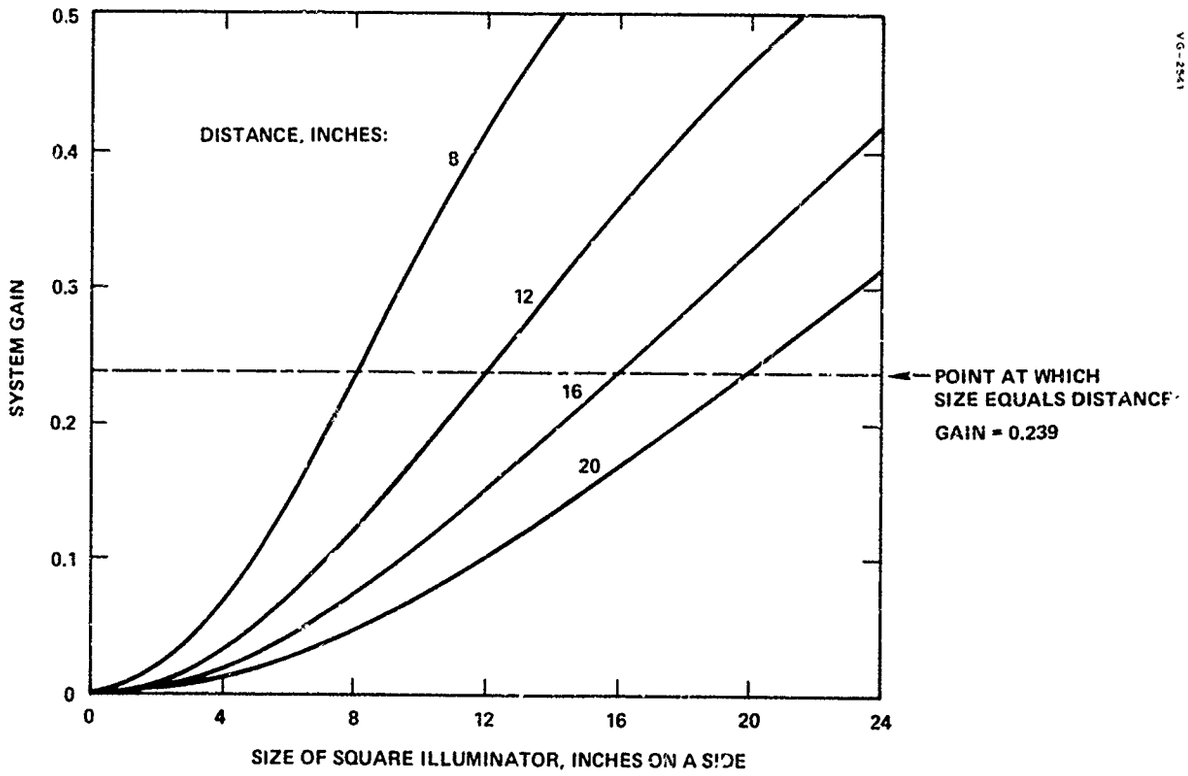


Figure 62. Efficiency of a square window related to that of a window of infinite extent. Parameter is distance of the window from the display surface.

luminance we can expect, then, assuming an illumination gain of 0. 24 and display maximum reflectance of 0. 20, is about 1. 4 x 10^2 cd/m^2 (40 foot-lamberts). At higher values of skylight, the figure approaches 5. 1 x 10^2 cd/m^2 (150 footlamberts). Any any sort of haze or cloud cover can be expected to increase sky luminance many times over this pessimistic value.

HEAD-UP DISPLAYS

There are two imaging schemes of interest for HUD or virtual-image displays: the light field and the dark field. In the light field scheme, the specularly reflected light off the liquid crystal display is used for producing the image, and the scattered light is blocked, and not used. In the dark field scheme, just the opposite occurs. The specular light is blocked out and the scattered light is used. This is shown in Figure 63. In the case of the light field, it is essential that the size of the aperture be kept quite small, since the contrast ratio will depend on how much of the scattered

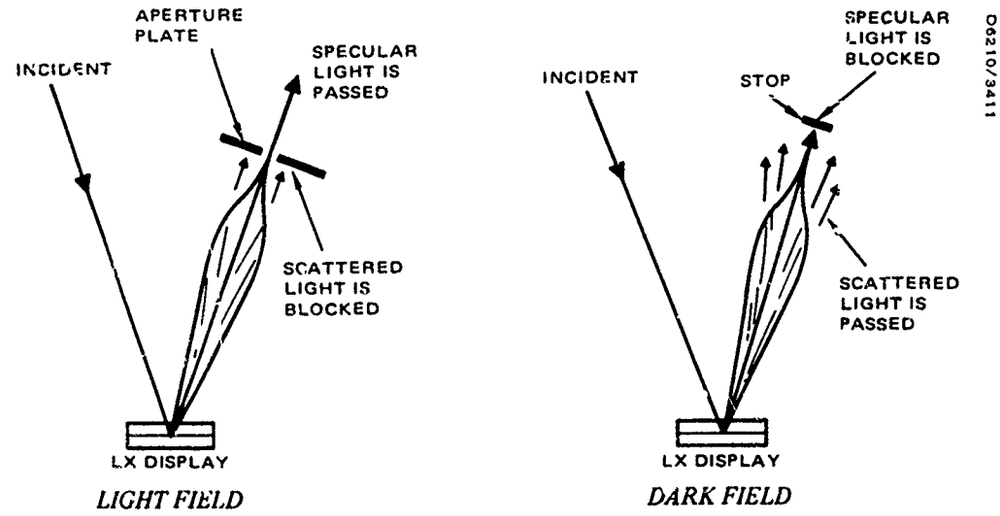


Figure 63. Imaging schemes using liquid crystal.

light is blocked. This is especially true since the liquid crystal is not an ideal diffuser and most of the scattered light is in the proximity of the specular reflection. This scheme is therefore much more difficult to implement within the normal optical constraints and performance requirements of a Head Up Display, and the dark field approach is considered preferable.

Dark Field Illumination ("schlieren")

When light is scattered by a surface such as the liquid crystal display, it is as though many tiny lenses acted to refract the rays in a random fashion, changing the phase but not the amplitude of the wavefront. Optical systems which respond to scattering or phase change have been used for making visible otherwise transparent bacteria under the microscope, and hard-to-detect striae, or bands, in optically ground surfaces. After the German word for striae, schlieren, they are commonly known as schlieren systems.

The basic principle of a schlieren system is to erect complementary stops at different points in the optical path, so that any direct ray which is transmitted by one stop will be blocked by the other one. The object to be viewed is placed between them and illuminated through the first stop. The only rays that will pass through the system to the observer are those which are deviated by scattering in the plane of the object; the latter thus becomes

a secondary source, located beyond the blocking stop at the entrance to the system. The observer sees this secondary source, which comprises only those rays which are scattered in the object plane.

Figure 64 shows the basic scheme of a schlieren optical system. Light coming from the left must pass around the entrance stop S1, which is actually a small disc. This stop is imaged by the optical system in the plane of S2, so that an undeflected ray (shown by the solid line) which has missed S1 must strike S2 and fail to pass through. To the degree, however, that these rays are scattered within the system, they will fail to form an image of S1 at S2, and will consequently fall anywhere within the S2 plane, including the aperture of the stop. If the scattering plane is located properly with respect to the second lens, the image formed by the scattered rays -- in this case, the liquid crystal surface -- will be visible to the observer.

The devices presently under development at Hughes utilize a reflective substrate. This allows the basic schlieren system to be folded about the plane of scattering, so that the two leases become one, and the complementary apertures can be provided by a single mirror. Figure 65 shows the same concept as illustrated in Figure 64, folded about the liquid crystal display. The mirror which transmits the scattered image to the observer

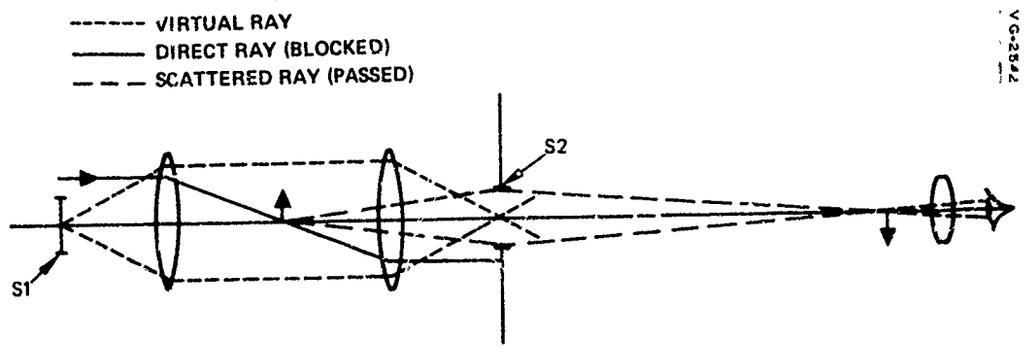


Figure 64. Basic schematic for schlieren optical system.

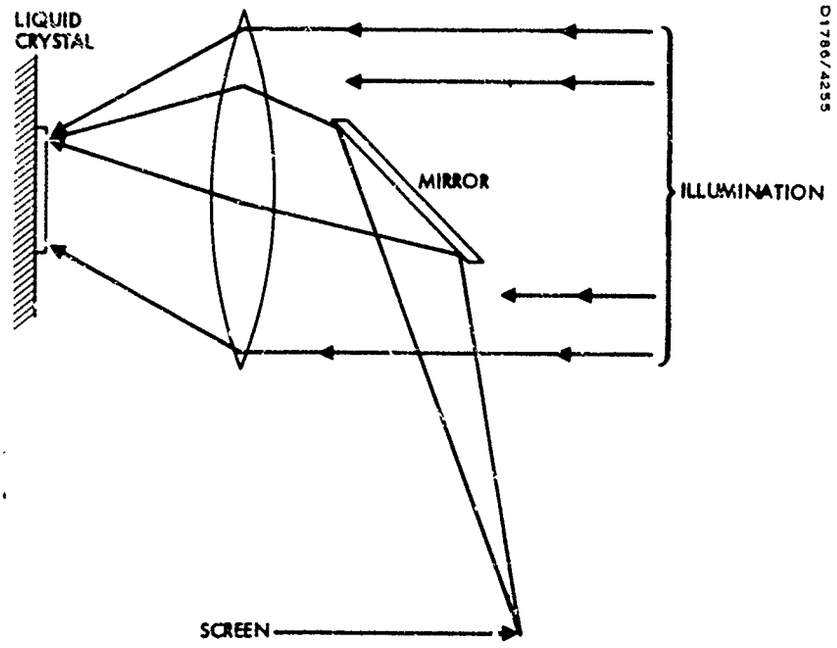


Figure 65. Design for a reflective schlieren display.

(in this case, a screen) serves as the S1 disc to incoming illumination; for the scattered light from the liquid crystal, it serves reflectively as the exit pupil, S2. Rays which have missed the mirror on entrance and are reflected without scattering by the liquid crystal surface, miss the mirror again on leaving and are not reflected to the screen (or to the observer).

Because a schlieren system is especially adaptable to projection, it is of interest to consider the utility of a rear-projected liquid crystal schlieren display in a typical cockpit environment. The following is assumed:

- Five-inch square screen at 30-inch viewing distance
- Lens 15 inches behind the screen
- Schlieren efficiency = 0.50 (Typical value for Hughes laboratory system)
- Liquid crystal reflectance efficiency = 0.20 (measured from actual cell)
- 10,000 footcandle ambient
- Required contrast of 1.0 (minimum)

It follows from the above geometry that the maximum bend angle between the extreme incident ray on the screen and the extreme viewing position is

14.2 degrees. With a 2-to-1 (3 decibel) uniformity requirement, a simple diffusing rear projection screen* can yield on-axis gain of 5.5 decibels with reference to Lambertian reflectance from a plane surface; the same screen will exhibit a reflectance coefficient of 0.10. We calculate the luminous output of a projection system capable of providing 1.0 contrast under 10,000 footcandle ambient under the foregoing conditions to be 320 lumens. This is approximately equivalent to the luminous output of a 300-watt home slide projector, indicating that such a system could be used for a cockpit installation.

The implementation of a schlieren dark-field system for a HUD requires that the specular reflection off the display surface be blocked while the scattered light is gathered. There are two basic approaches that are feasible, one for on-axis display viewing (display normal to optical axis), and one for off-axis viewing (display tilted).

On-Axis Viewing

The on-axis approach consists of a schlieren optical arrangement as shown in Figure 66. Light from the source is imaged onto a small diagonal mirror on the optical axis at the focal point of the field lens. This becomes a point source and is collimated by the field lens so that the incident rays are normal to the display. The specularly reflected rays are folded back on the incident rays and are focused by the field lens back onto the diagonal mirror which now acts as a stop and prevents them from entering the relay

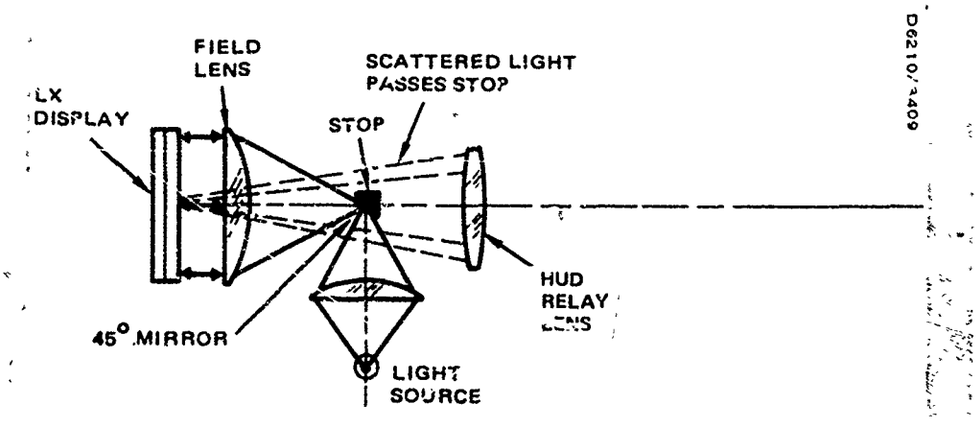


Figure 66. On-axis schlieren system.

*Nonlenticular - "frosted" Mylar film or Opal glass.

lens. Scattered light from the liquid crystal will not be normal to the display and therefore will miss the stop and reach the relay lens.

While this system seems ideal for gathering the scattered light from the liquid crystal, it suffers from several drawbacks. In the first place, the light is gathered from narrow angles around the specular reflection, determined by the size of the stop. These angles contain unwanted dispersed and scattered light from the display surface, and limit the contrast. If the size of the stop is increased to block off a greater angle, the effective gathering area of the relay lens will be reduced and brightness will fall off. Furthermore, an image of the stop will appear at the exit pupil, thereby creating an undesirable "hole" proportional to the size of the stop. This system is therefore considered inappropriate for application to the HUD.

Off-Axis Viewing

A second approach utilizes an off-axis viewing system where the display is tilted with respect to the HUD optical axis. Light sources are situated around the display such that their specular reflections off the display cannot reach the relay lens, but the light scattered from the liquid crystal can. Because of the non-uniform scattering lobe of the liquid crystal, it is advisable to use two light sources for greater uniformity, as shown in Figure 67. By placing the light sources at the proper angles, it is possible to maximize the brightness and contrast of the display to give the best overall performance.

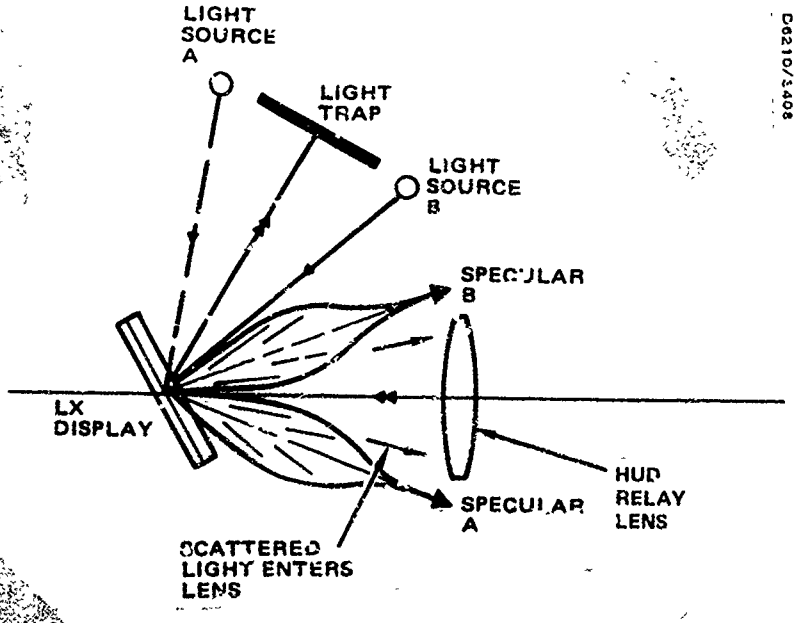


Figure 67. Off-axis viewing system.

It is expected that this approach will yield the best results for a HUD application. The liquid crystal performance can be optimized, and the requirements on the light sources and optical system can be relaxed. This allows greater flexibility in the design and manufacture of these components.

Special Lighting Considerations

Because of the wide dynamic range of background brightness normally encountered with Head Up Displays, it is desirable to control the brightness of the display over a similar dynamic range, thereby maintaining a reasonable contrast ratio. The types of light sources currently feasible in this application have a controllable dimming range of approximately 10/1. An alternate method is therefore proposed that uses two linear density wedges in front of the light source, as shown in Figure 68. As the two wedges slide past each other over the light source, their optical density changes, thereby controlling the apparent brightness of the light source. Such wedges frequently have a dynamic range of 10^3, and using two wedges sliding in opposite directions provides more uniform attenuation with a maximum dynamic range of 10^6.

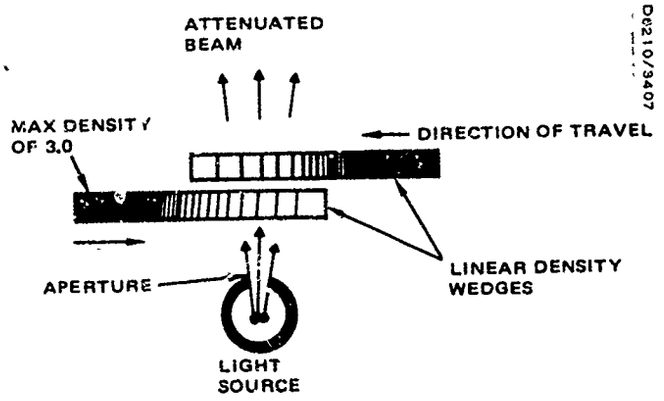


Figure 68. Light source brightness control.

Holographic HUD Light Source

In a head up display, the symbology highlights are viewed against a 10,000 fL background brightness which has a dynamic range exceeding 1,000,000 to one. The utilization of a holographic optical combiner in a HUD system demands that the image source be narrow in bandwidth. A hologram which has to act upon a broad-band light source would have low efficiency and block out a large portion of the light coming from the outside

world. This blockage not only attenuates the light coming from the outside world, but colors it as well. In order for a narrow band illuminating source to have maximum efficiency, it should have a wavelength which lies relatively close to the peak of the average eye sensitivity; around 555 nm. Optical filters are available which are capable of filtering out unwanted wavelengths from broadband sources rendering them spectrally narrow, however, the efficiencies associated with this type of illumination technique are drastically lower than that which would permit a reasonable power input to the display.

In summary, the requirements of an illuminating source to be used with a liquid crystal display for a Holographic HUD are: high brightness, narrow bandwidth, compact geometry, and good efficiency.

The brightness requirement for the illuminating source is determined as follows. We use as a baseline assumption a sky background (cloud) luminance of 3.4×10^4 cd/m^2 (10,000 foot-lamberts), which is seen through a holographic combiner as 3.1×10^4 cd/m^2 (9000 foot lamberts) because of the 90 percent efficiency of this element to the transmission of ordinary light. The projected light forming the symbols is added to this background, so if these symbols are to show a contrast ratio of 1.2 against the background the projected symbol luminance, as seen by the operator, must be $0.2 \times 3.1 \times 10^4$ or 6.2×10^3 cd/m^2 (1800 foot-lamberts). In the optical system of the HUD, this corresponds to a highlight brightness at the source of about 8.9×10^3 cd/m^2 (2,600 foot-lamberts) when system transmission of about 70 percent is considered. Assuming an average scattering efficiency of 100 percent by the display surface, an illumination flux of 2.8×10^4 flux (2,600 lumens/ft^2) will be required. Since the display has a dimension of about 3.5 inches, a 12 in^2 area must be floode , therefore, about 1/12 of 2,600 or 220 lumens is required from the light source.

For advanced HUDs, an improved contrast ratio of 1.8:1 is desired, resulting in a light source of 800 lumens for a 12 in^2 area; a feasible value for high intensity illumination sources.

Source Tradeoff

The candidate light sources must have high efficiency in a narrow band (~2 nm) centered near the peak of visual sensitivity (~555 nm). Broadband radiation is considered to be inappropriate because of low-efficiency, however, the tungsten lamp will be discussed briefly. Three other classes of lamps are also discussed which are more appropriate as sources: they are: gas discharge, solid state and excited phosphor lamps.

Incandescent Lamps. The spectral energy distribution of an incandescent lamp closely approximates a black body radiation spectrum. At a color temperature of 3800°K, a practical maximum for this type of lamp, the fraction of radiant energy within a 2 nm band centered at 555 nm is 0.03 percent. Optical filtering efficiency is about 50 percent so that the total power required to achieve reasonable output from the source would be astronomical. The incandescent lamp is therefore not practical for this application.

Gas Discharge Lamps. The first class of non-incandescent lamps considered produce a narrow spectral emission band of gas discharge. A variety of lamps are manufactured to generate narrow spectral bandwidths at various wavelengths. These glow discharge lamps emit a characteristic glow corresponding to the arc discharge characteristics of the element in the cathode. One such lamp manufactured by Westinghouse has a thallium cathode which emits a strong line at 535 nm, a wavelength suitable for this application. The 535 nm line is at about 90 percent of visual response. Thallium iodide arc lamps have been built recently for narrow band illumination in oceanographic research. Currently manufactured arc lamps are approximately 5 percent efficient in the required 2 nm bandwidth at 535 nm.

Solid-State Illuminants. The second class of lamps to be discussed is solid state devices. This includes light emitting diodes, electroluminescent panels, and solid state lasers. Solid state light emitting diodes (LEDs) have been manufactured for some time, but efficient materials have not been found for operation in the 555 nm portion of the spectrum. The best green LED is made from gallium phosphide and has been reported to produce efficiencies of approximately 0.1 to 0.6 percent in a 250 Å bandwidth. If the

entire panel were to be illuminated uniformly from LED sources, a large number of devices would be required. With possible efficiency of 0.5 percent large input power would be required.

Electroluminescent panels are radiating devices that are fabricated as a sandwich structure with a phosphorescent material between two electrodes. The process is very inefficient due to the high fields required for ionization. An example of a state-of-the-art device would be an electroluminescent panel consisting of a ZnS:Mn, Cu phosphor panel, operating at 100 VDC and 2.5 ma per cm^2 power input with a 3.4×10^2 cd/m^2 (100 foot-lambert output). The conversion efficiency is 0.1 percent, but the radiated output is in a 50 nm bandwidth (at a peak wavelength of 580 nm). The brightness and efficiency is far below that required for this application.

Solid state lasers might be considered for application to holographic HUDs, since they are more efficient than light emitting diodes or electroluminescent panels. Their operating conditions, however, are not favorable for a practical airborne display. The materials require cooling to cryogenic temperatures to emit the characteristic high energy, narrow band radiation.

Conventional phosphors excited by an ultraviolet photon beam are a third class of light sources considered. Photoluminescence is the process of converting photon radiation of one wavelength to photon radiation at another wavelength. The conversion of interest is from the ultraviolet radiation of the mercury arc at 253.7 nm to the photoemission of visible light near the 555 nm peak of visual sensitivity. The efficiency of the 253.7 nm source and the conversion efficiency of the phosphor are both quite high, yielding a high overall luminous efficiency. Light sources using phosphors, however, tend to be line sources or area sources rather than point sources, and it is therefore more difficult to condense or collimate a light beam. The requirements of the illumination system must determine whether this type of source can be used effectively.

A summary of the various light sources is given in Table 9. The relative efficiencies of the sources are listed as well as the estimated power requirements to obtain the desired light output.

Conclusion. From the data in Table 9 it can be seen that only two light sources are practical for this application — the thallium arc lamp and the mercury arc-phosphor lamp. Of these two, the mercury arc-phosphor lamp

TABLE 9

CANDIDATE LIGHT SOURCE TECHNOLOGIES FOR HOLOGRAPHIC HUD

Lamp Type	Efficiency 20Å Band	Efficiency 100Å Band	State of Development	Power Required 20Å	Power Required 100Å	Relative Cost	Wavelength	Notes
Solar System							Broad	Complex servo system required for tracking/Nighttime illum required.
Tungsten Lamp	0.03%	0.15%		40KW	8KW	Low	Broad	Inefficient Not Applicable
Laser $CdS_{(x)}CdSe_{(1-x)}$	~12%	~12%	Research	80W		High	Any Available	50KV electron excitation/ Undesirable cryogenic cooling
Electro-Luminescent	0.006	0.03%	Research	Astronomical			580 nm	Inefficient/ Not Applicable
Thallium Arc Lamp	~5%	>15%	Within State of Art	120 W	40W	Low	535 nm	Point source. Power supply required. Collimator required.
Mercury Arc and Phosphor	25%	40%	Laboratory	50W	35W	Low	544 nm	Diffused source. Power supply required.
Electron Beam Activated Phosphor	1.6%	3.3%	Laboratory	1200W	600W	Med.	544 nm	20KV electron excit. (Power assumes 50% CRT gun efficiency)
Light Emitting Diode	0.15%	0.5%	Production	12KW	2.5KW	High	Several Alt (one at 550 nm)	Good for discrete point illumination

is the more efficient and is therefore the best choice for the HUD application, since a line source is permissible in the illumination system. The brightness and spectral requirements for this lamp make it rather unique, however, and no lamp of this exact type is currently being manufactured. It will therefore be necessary to undertake a lamp development to meet the requirements of this application. The design of such a lamp is a straightforward application, however, and is discussed in the next section, including a development of the anticipated power requirements and a description of the mechanical configuration.

Design of a Special Purpose Mercury Arc Phosphor Lamp

Choice of Phosphor. The design of a special purpose phosphor lamp for use with holographic optics will be similar to the design of a conventional fluorescent tube except for the type of phosphor that is used. The ideal phosphor for this application should emit all its energy in a very narrow band at the 555 nm peak of visual sensitivity. Of the current phosphors available, the one that comes closest to this requirement is P44, normally used for special purpose CRTs. The spectral characteristics for the P44 phosphor are shown in Figure 69. The peak output occurs at 543.2 nm, which is at 97 percent on the visual sensitivity curve. Most of the output energy is

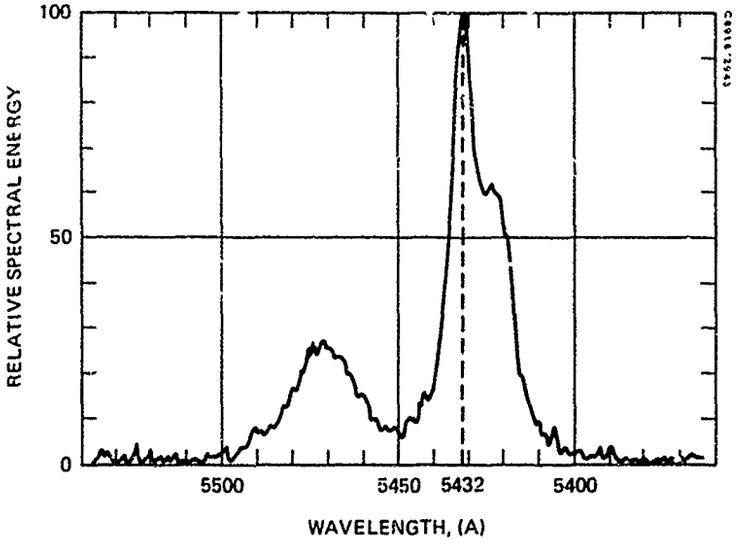


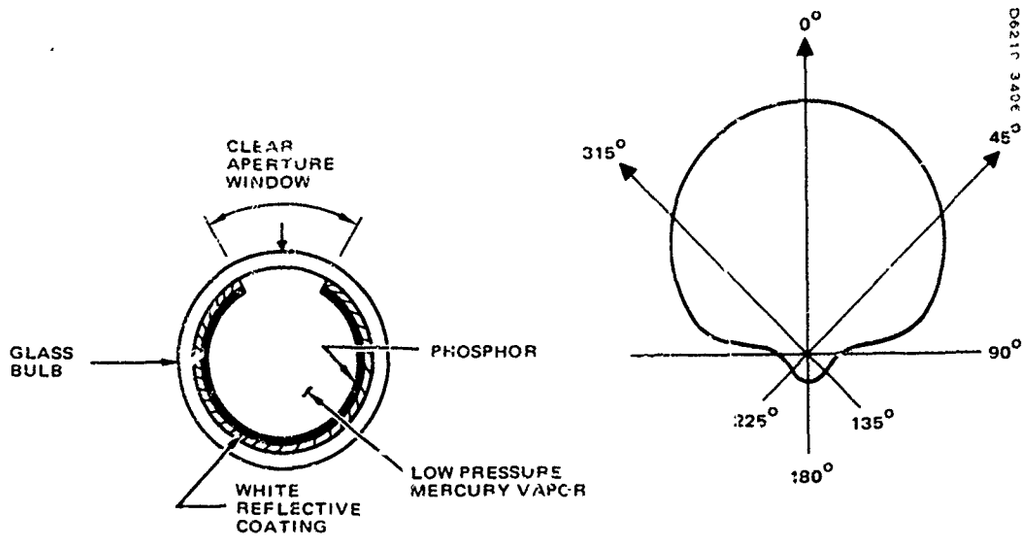
Figure 69. Measured spectral response of P-44 phosphor.

contained in a band about 2.5 nm wide, making it ideally suited for use with holographic optics. This phosphor is a burn resistant phosphor normally used in high brightness CRTs, and can also be excited by UV radiation at 253.7 nm from a mercury arc. It is considered to be the best phosphor for this application. P-43 phosphor has the same spectral output and may also be used.

Bulb Design. The basic construction of the lamp consists of a glass tube coated with the desired phosphor on its inside surface. End caps containing electrodes are placed over each end, and the entire tube is then evacuated and filled with low pressure mercury vapor. A voltage placed across the ends of the tube will draw an arc through the mercury vapor, which emits UV radiation at 253.7 nm. The phosphor on the inside of the tube absorbs this radiation and emits light in the visible portion of the spectrum. With a P44 phosphor the light output will be at 543.2 nm.

The efficiency and output characteristics of the lamp depend on bulb diameter, arc length, and radiation pattern. The efficiency of the bulb generally increases as its diameter and length increase. The limiting factor in this case is the size constraint imposed by the package dimensions, which limits the length to about 6 inches. The bulb diameter can be as large as 1-1/2 inches, which is about the optimum for efficiency. Since radiation from the bulb is not required in all directions, a special construction technique can be used to greatly increase its radiation pattern in the useful direction. This is shown in Figure 70. A clear window is left on one side of the bulb and the rest of the interior is coated with a white reflective material. The phosphor is then placed over this reflective material and the bulb is filled and sealed. As a result, the inside of the bulb acts somewhat like an integrating sphere, with most of the light being internally reflected until it exits through the aperture window. The light output of this lamp can be up to 10 times the output of a standard fluorescent lamp in the direction indicated by the radiation pattern.

Anticipated Results. The performance of the special purpose P44 lamp can be estimated by scaling up the performance of a standard fluorescent lamp. A normal CW (cool white) fluorescent lamp with a 12.7 cm (5 inch) arc length will put out about 35 lumens/watt. The luminous efficiency of the



SPECIAL BULB CONSTRUCTION *RADIATION PATTERN*

Figure 70. Mercury arc-phosphor lamp.

the CW phosphor is about 51 percent, compared to over 90 percent for the P44 phosphor. Assuming that UV to visible conversion efficiency of the phosphor is about the same, the output of the P44 bulb should be around 65 lumens/watt.

It is assumed that the gathering efficiency of the proposed illumination system will be approximately 20 percent. Thus a holographic HUD will require an incident flux of 800 lumens, and therefore the bulb output should be approximately 4000 lumens, assuming it radiates equally as a line source in all directions. If the special construction technique yields a radiation pattern that has a gain of only 2 to 3 times, it essentially increases the gathering efficiency and lowers the bulb output requirement to 1300-2000 lumens. At an efficiency of 65 lumens/watts, this corresponds to a bulb power in the range of 20 to 30 watts. A special power supply will be required to drive the bulb, and including its efficiency (ballast losses, etc.) in the calculations, the total power will remain less than 50 watts for a holographic HUD exhibiting 1.8 contrast and approximately 25 percent of this value for 1.2 contrast, the latter being the value obtained from current state-of-the art HUDs.

SECTION V

LARGE SCALE INTEGRATION FOR DISPLAY ADDRESSING AND ELECTRICAL INTERFACE

A matrix display with sufficient resolution to display pictorial information would find only limited application without an economical means to multiplex the connections to the individual row and column electrode busses. The circuits required to perform this function are referred to here as drive circuits, and a review of the work that was done toward their design follows. Functionally, the drive circuits serve as an interface between the matrix display surface and the communication channel supplying the data to be displayed. The advantage of using a semiconductor addressed liquid crystal display is that its voltage and impedance levels are compatible with the drive capability of the present state-of-the-art microminiaturized integrated circuits. The impact of microminiaturizing the drive circuits with an LSI circuit approach is graphically illustrated in Figure 71.

FUNCTIONAL REQUIREMENTS

Line-at-a-Time-Addressing

In conventional television systems, one video channel carries all the pictorial information in a serial analog data format. The camera (sensor) scans the scene from the upper left hand corner along the top horizontal line from left to right. One scan from top-to-bottom of the picture area is defined as one field. A second field is then drawn beginning at the upper left-hand corner; but, these lines are interlaced between the previously drawn lines. Together the two fields form an interlaced frame of pictorial information. The deflection system in a conventional CRT television display effectively causes the scanning beam to continuously address from the picture as the beam progresses through a predetermined scan pattern (raster).

In the liquid crystal airborne display, addressing is an X-Y matrix function in which a bidirectional field-effect transistor (FET) is used as the active switching element at each and every X-Y intersection. A circuit diagram of the addressing circuits contained within the basic

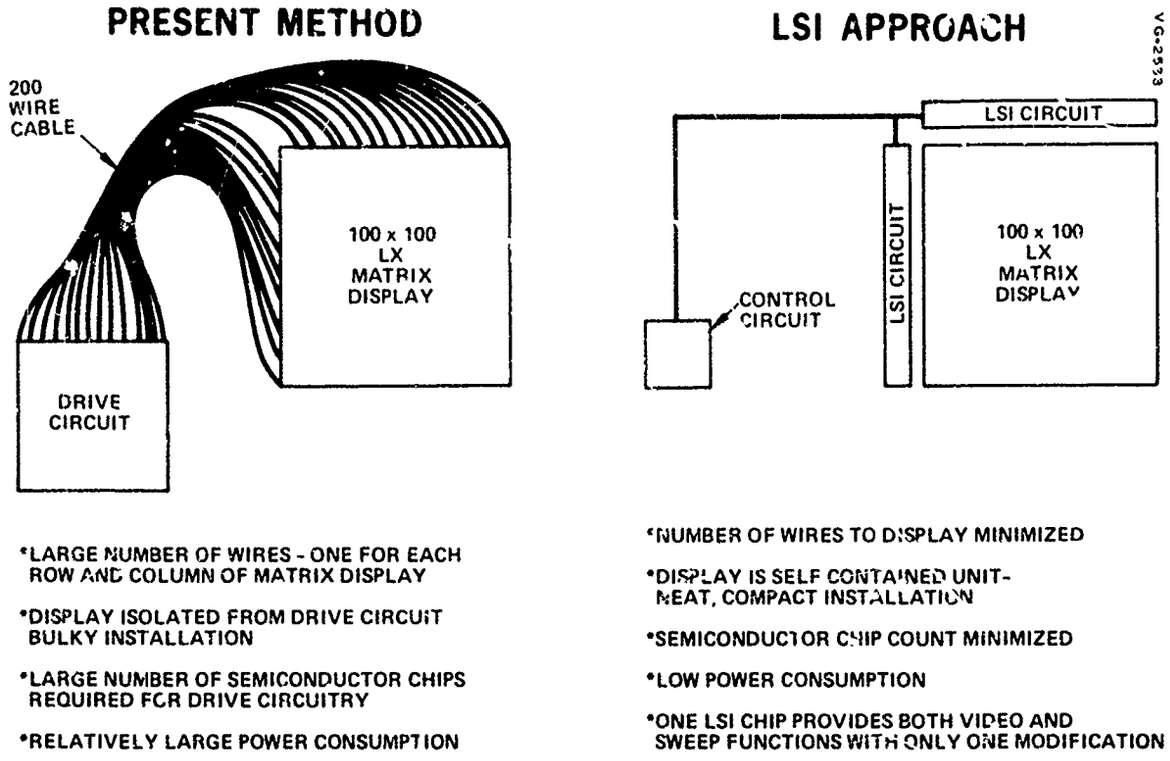


Figure 71. Advantages of LSI driving circuits.

electrode-array chip was previously described and shown in Figure 12. The waveforms shown in Figure 7[illegible] illustrate the operation and the relationship between the applied video electrode bus signal voltage and the scattering level of the liquid crystal material. The waveforms are shown for two conditions occurring during three sequential TV frames: (1) where the video signal being sampled does not change, and (2) where the video signal being sampled decreases and then increases. In each frame, when the element is addressed the capacitor voltage rises or falls to the new value in a matter of microseconds; the changes in liquid crystal material scattering level occur much more slowly. The voltage applied to the liquid crystal material remains essentially unchanged in the 33 millisecond period between addressing intervals. Thus, the speed-of-response of the display image is primarily influenced by the response of the liquid crystal material to d.c. excitation.

This circuit has the advantage that it is the simplest circuit that can perform the required addressing function, but it is the nature of this circuit to require that the display be addressed a line at a time. In line-at-a-time addressing, the new data for an entire line is written in simultaneously.

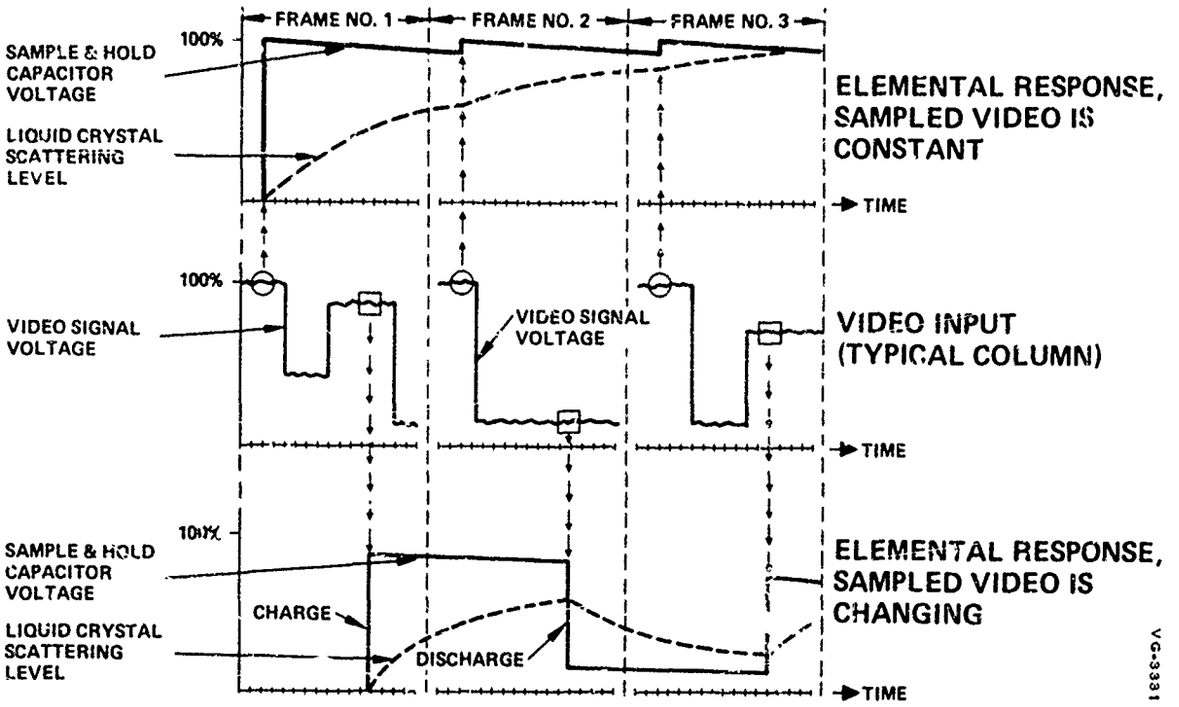


Figure 72. Idealized time response of display.

This addressing arrangement is not directly compatible with conventional television systems where the data are in a serial time format rather than a parallel line format. Thus, each serial line of television analog video data must be converted to parallel data for simultaneous presentation to a line of liquid crystal picture elements. This demultiplexing function can be performed by a dual serial/parallel analog converter.

Video information from the serial/parallel analog converters is provided, in parallel, to each column of the matrix and is updated in synchronism with the sweep multiplexer. Thus, each picture element along a line is provided with new and unique video information during the time interval normally allotted to one television horizontal line period (including the blanking interval). The line-at-a-time scan proceeds sequentially from the top to the bottom in two alternating fields. In the odd field, the odd-numbered lines are written. Together, the odd and even-numbered lines constitute a full frame of pictorial information.

Sweep Circuits

Referring back to Figure 12, the line-enable signal, which commands each of the lines in sequence, is analogous to the vertical sweep function required for television raster scan. The function labeled sweep circuit shift register in Figure 11 is implemented with a serial-input/parallel-output shift register which has an associated driver circuit for each line of the display. One bit in the shift register corresponds to the address of one line (gate bus), and a single ONE in a field of ZEROS is shifted through the register to cause the lines to be sequenced (swept) in the vertical dimension.

The voltage level to which each gate line must be driven to turn on all of the FETs in that line of the display, i.e., the minimum amplitude for the enable signal, is determined by threshold characteristics of the FET switches formed as part of the electrode array chip and the characteristics of the liquid crystal material with which the display is filled. A circuit schematic for an elemental cell is shown in Figure 73, and the gate voltage that must be applied to turn on the FET of the elemental cell as a function of drain and source voltage is plotted in Figure 74. The threshold voltage (the extra voltage increment by which the gate-to-substrate voltage must exceed the drain/source-to-substrate voltage in order to hold the FET "ON") increases with increasing drain-to-source voltage due to the tendency of the higher drain-to-source voltage to "pinch-off" the FET. The voltage level to which the drain-to-source must be driven to fully saturate the liquid crystal material is typically 20 volts and is determined by the electro-optic transfer function of the specific material that is used (see Figure 40). Thus, to excite the liquid crystal material to nearly full saturation, a gate-enable pulse amplitude of approximately 28 volts (material threshold + FET threshold + saturation value) must be used.

The width, repetition rate, and rise and fall times of the enable signal pulses are determined by the rate at which new lines are to be written on the display and the tolerance on adjacent element cross talk. The data transferred to an individual picture element on the display consists of an analog sample of the video signal, plus an enable-signal pulse to control the timing of that sampling process. If the sampling interval is too short, there may be insufficient time to fully charge the elemental storage capacitor; if it is too long, there will be an overlap between samples and a loss of vertical

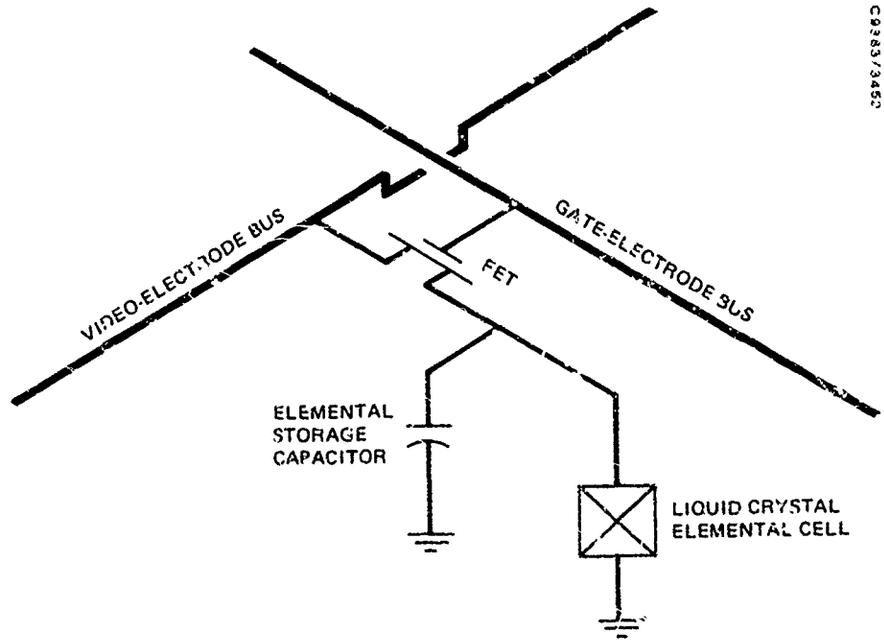


Figure 73. Circuit schematic for elemental cell.

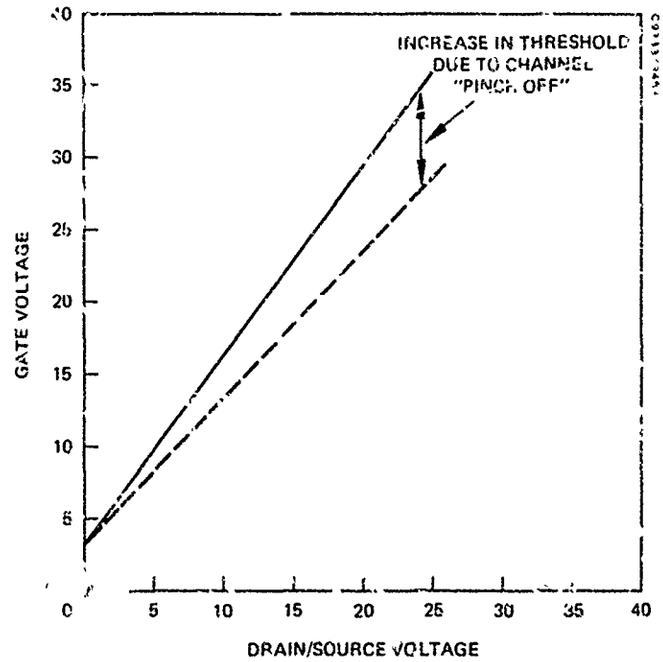


Figure 74. Effect of pinch-off on threshold.

resolution. For an RS170 standard television signal, the horizontal line rate is 15.750 kHz; hence the ideal width for the enable pulse is 63 microseconds.

Video Circuits

Line-at-a-time addressing requires that all columns of the display be driven in parallel with separate and distinct video signals. When the video data source is a conventional standard TV signal whose data are in a serial format, the necessary video signals can be derived from the input signal by performing a serial-to-parallel conversion. The serial-to-parallel conversion of analog video is analogous to the serial-to-parallel conversion of digital data, but different in that the magnitude of the signal must also be preserved. Dual serial-to-parallel video converters, alternating their functions, can collect the serial data while simultaneously outputing previously collected data to a line in parallel form. The sweep function is performed digitally by a simple shift register propagating an 'enable' pulse to determine which line is written. The updating of the video data is stepped in synchronism with the shift register.

A serial/parallel converter takes sequentially presented data and stores it in a series of data bins that can be interrogated in parallel. The simplest serial/parallel analog converter consists of a set of sample-and-hold circuits with one sample-and-hold circuit for each of the parallel output channels and a shift-register to cause the sampling function to be enabled sequentially, thereby providing a sample and hold function for each picture element along a line.

Assessing of the accumulated data requires that there be a pause in the accumulation (sampling) process while the video is being applied to the line of pixels. These pauses would result in a loss of video data, for there is no provision in a real-time display for pauses to occur, unless they can be accommodated during the inactive line-blanking-interval. This interval is impractically short for standard RS170 television signals. A better scheme is to use two converters (see Figure 75) in an alternating read-write sequence. In this manner one converter is sampling video during the entire time the other converter is outputing data to the line.

The rate at which the serial video data must be sampled and stored depends upon the number of picture elements per line in the matrix display. In the case of a matrix display driven from an RS170 standard 525 line television signal source, the display has equal vertical and horizontal resolution

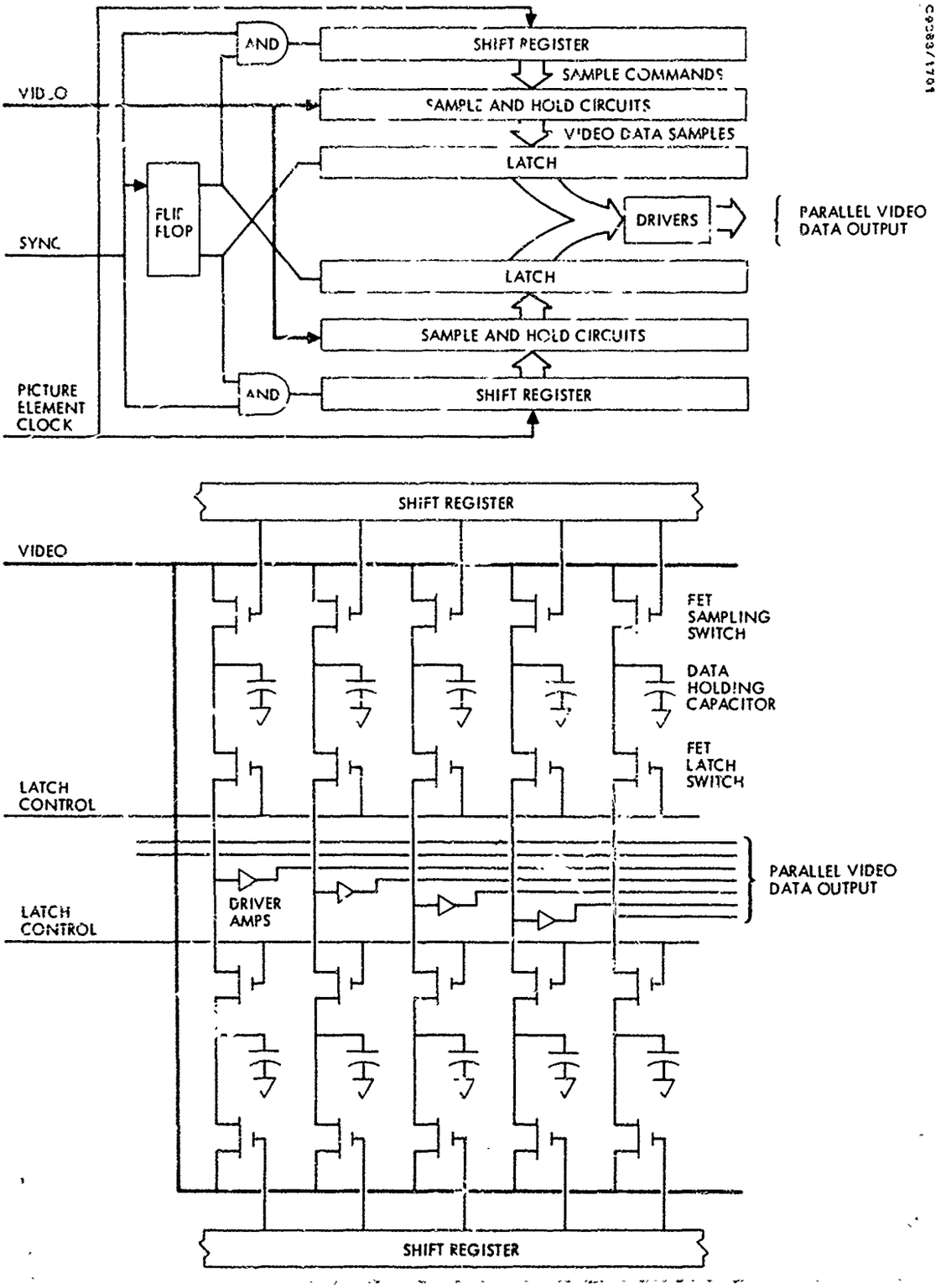


Figure 75. Typical serial/parallel video converter.

density, while the signal does not. The sampling rate in MHz is given in equation 8.

$$\frac{\text{Active horizontal line interval}}{\text{No. of active vertical lines x Aspect Ratio}} = \frac{52 \times 10^{-6} \text{ secs}}{480 \times \frac{4}{3}} = 12.3 \text{ MHz} \qquad \text{eq. 8}$$

The magnitude of the video signal applied to the column electrode bus is a function of the specific liquid crystal material being used and the alignment technique as previously discussed. Typical characteristics of the liquid crystal matrix display employing the semiconductor drive chips being fabricated at the present time call for:

- Video signals that are negative going with respect to ground.
- The magnitude of the video signal should be linearly proportional to the input video signal, except when gamma correction is provided.
- Typically 15 to 20 volts is needed to saturate the liquid crystal material.
- The video signal must be prevented from going positive.
- The video signal black level should be lower than the threshold of the liquid crystal material which is typically in the range of three to five volts.
- The transition of the video signal from one level to another should be short compared to the 63 microsecond line time.

The impedance of the drivers should be such that the required waveforms are maintained when driving 200 pico farads per inch of display. The leakage currents are insignificant.

Design Constraints Associated with LSI

LSI circuit design requires a complex series of trade-offs between switching speed, operating voltage, and the number of electrical connections per chip, among other factors, and the results influences not only the electrical and mechanical layout of the circuit but the semiconductor processing sequence as well. External multiplexing circuitry can be avoided if the integrated circuit chips can sample the input video at the required 12 MHz rate. A high operating voltage is needed, because a 20 volt signal capability is required to drive the video electrode busses and almost 30 volts is required for the enable signal pulses. The ability to have many electrical connections to each chip (pin-outs) is advantageous because restrictions on circuit partitioning are reduced.

There are presently many more basic alternative processing approaches suitable to the fabrication of LSI circuits than there were in 1974 when the design of the LSI drive circuits was begun. P-channel MOS (P-MOS) is the most mature LSI circuit technology, and it is now the most popular because its comparatively simple processing leads to higher yields and hence lower costs. N-channel MOS is rarely used by itself because it offers no advantage over P-channel MOS, and the processing is more difficult. Complementary MOS or CMOS has only recently come into wide use and it is normally used in applications where its expense is justified by the very low power drain. Bi-polar LSI is also a recent innovation, and it is generally chosen where very high speed is required. The last alternative, charge-coupled devices (CCDs) have a unique potential advantage for use in the liquid crystal pictorial display; the many components required to perform the serial to parallel analog signal conversion could be replaced with an analog CCD shift register. However, in many respects the CCD is still a developmental device.

In 1974, P-Channel MOS was chosen as the best suited process for implementing the custom LSI drive circuits for the liquid crystal pictorial display for the following reasons:

(1) Its 3 MHz to 5 MHz data rate is sufficient;

(2) It can operate from a higher power supply voltage (30 volts) than any of the others with standard processing; and

(3) The mature state of its technology minimizes the risk associated with developing a complex LSI circuit.

This conclusion still seems correct today, but it is going to need re-evaluation as the CCD technology matures. A CCD and C-MOS combination on a single substrate could prove to be an attractive alternative.

Design Approach

It is not necessary to design separate circuits for the sweep and video drive functions as the serial to parallel converter used for the video drive can also provide the correct sweep drive signals with the addition of simple external circuitry. The action of the shift register normally envisioned for the sweep drive function can be simulated by inputing to the "video input" of the serial-to-parallel converter a synthetic video signal consisting of a single pulse which is one sample interval in width and delayed from the previous pulse by N+1 sample intervals, where N is the number of lines on the display. When the serial-to-parallel converter for the sweep function is clocked at the same rates as the converter for the video function, and a synthetic video signal is provided as described previously, all of its outputs will be low except one, and that one will step in position by one-line during each horizontal line interval. In this manner one can provide a drive chip that performs double duty.

In the design of the circuit to perform the serial-to-parallel analog conversion, the decision concerning the relative placement of the amplifiers and multiplexers is crucial. If the signal is amplified first and then sampled by the multiplexer, it is very difficult to build a multiplexer that will operate at the required speed. Semiconductor devices have a speed-power product

limit that dictates higher power for higher voltage operation unless the capacitance of the circuits can be simultaneously reduced. If the signal is sampled at a low level and then amplified, it is necessary to build many amplifiers, and it is very difficult to build totally integrated linear amplifiers that are closely matched in performance. A third alternative is the multiplex-amplifier-multiplex configuration used for the discrete component drive circuits, but it too is not without difficulties. The outputs of the slow speed multiplexer are not in the correct time-space relationship. (For example, the outputs of the first slow speed multiplexer may be timed for driving lines 1, 9, 17, 25, ...), and a complex printed circuit board is required to reorder their connections to the other display drivers.

The design approach that was chosen for the custom LSI circuit chip, but which has not as yet been implemented, has a low level multiplexer followed by an amplifier for each output as illustrated in Figure 76. The approach was designed in detail, (see Figure 77), and a layout was drafted, (see Figure 78). It was concluded, based upon this detailed design work, that it was best to partition the circuit such that each chip would drive 16 lines of the display. Increasing the number of driven lines results in too large a chip, and decreasing the number of driven lines results in more connections for control than for outputs (see Figure 79).

A computer simulation was performed on the aforementioned custom circuit design, and it was concluded that the linearity required for operation as a video driver and the high voltage required for operation as a sweep driver could not be obtained from the same chip. However, the same basic design could be used, and the end use would be determined by the final metallization as illustrated in Figure 80. The performance anticipated from this design is given in Table 10.

Expansion to Larger Display Formats

A goal of the custom large-scale integrated drive circuit design effort has been to obtain a single integrated circuit chip that would efficiently drive the single module, 100 x 100-pixel display, the quad module 200 x 200-pixel display, and the not yet developed 500 x 500-pixel display, from an RS170 standard 525 line television signal. The difficulty was that the rate at which

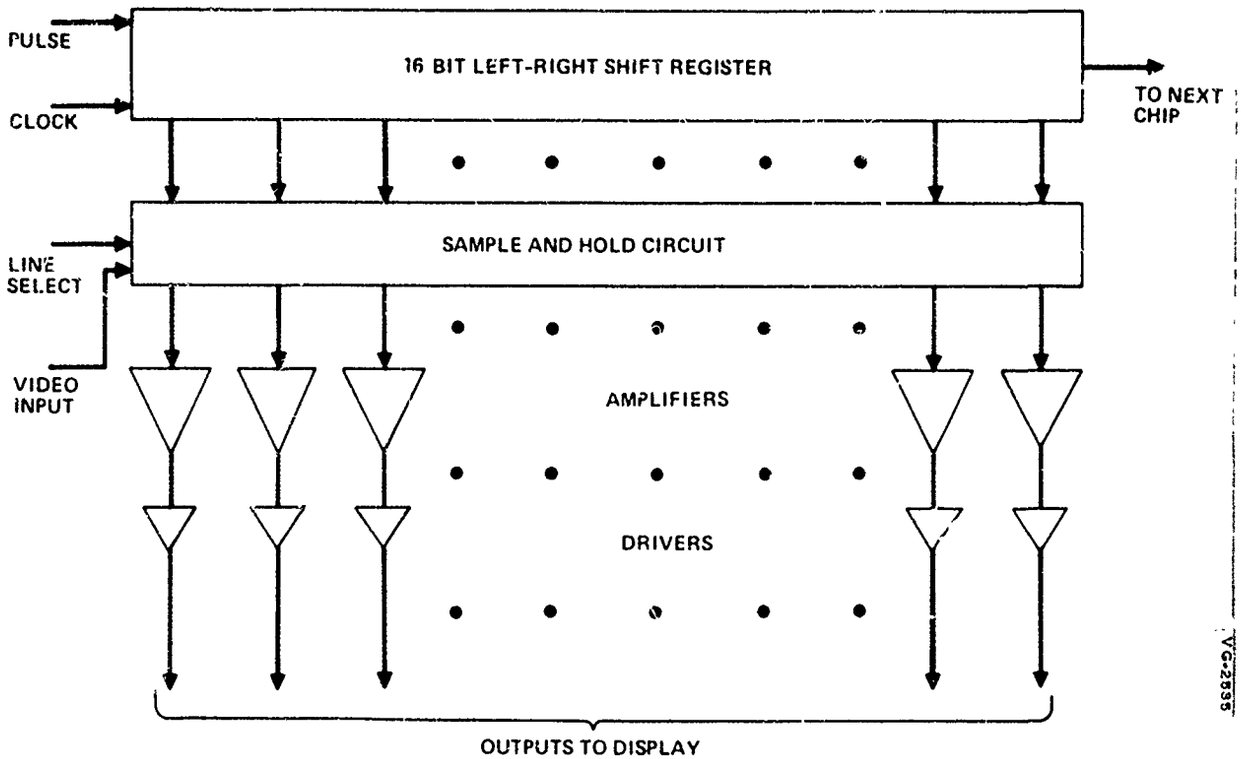


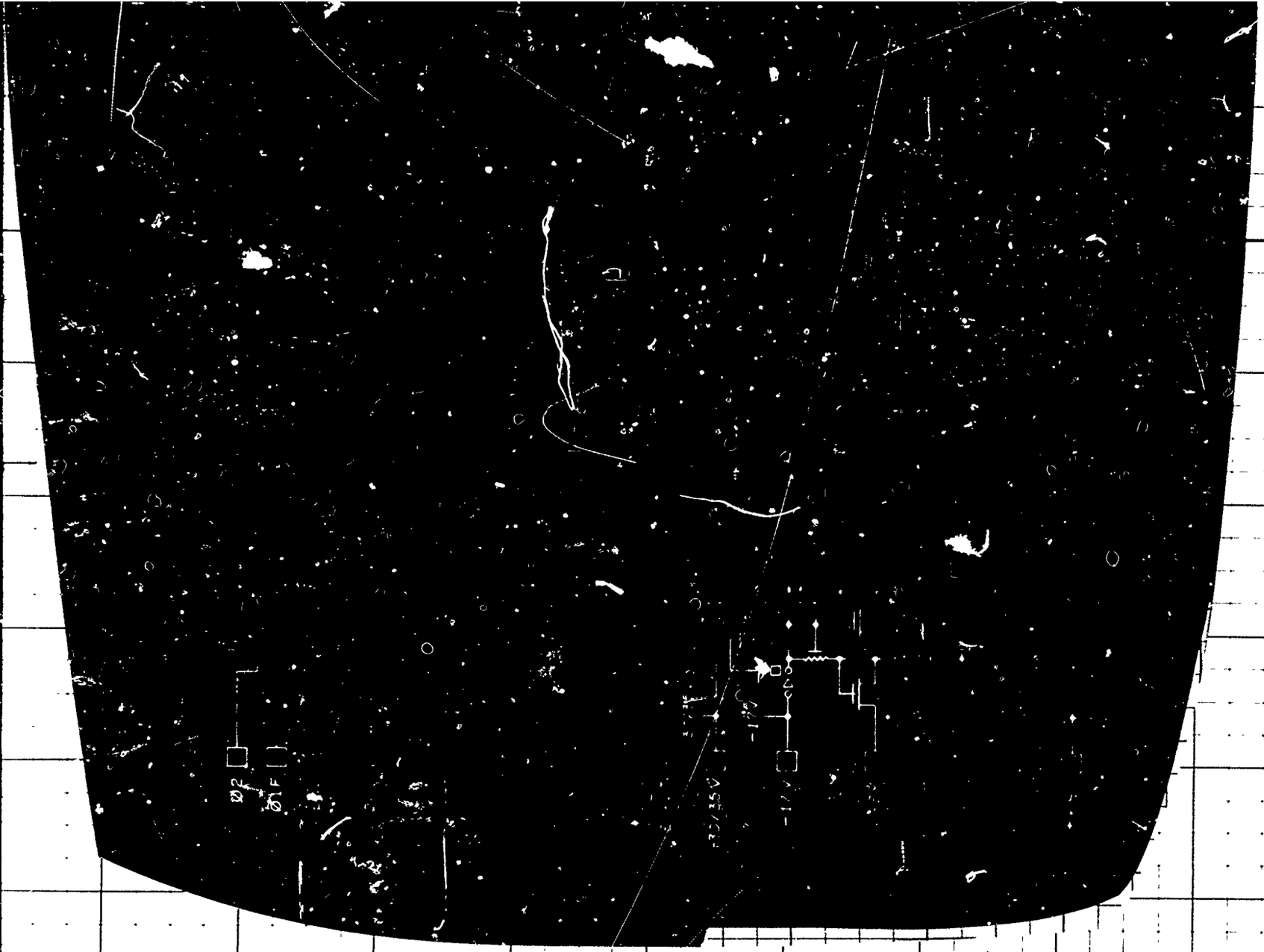
Figure 76. LSI drive circuit functional block diagram.

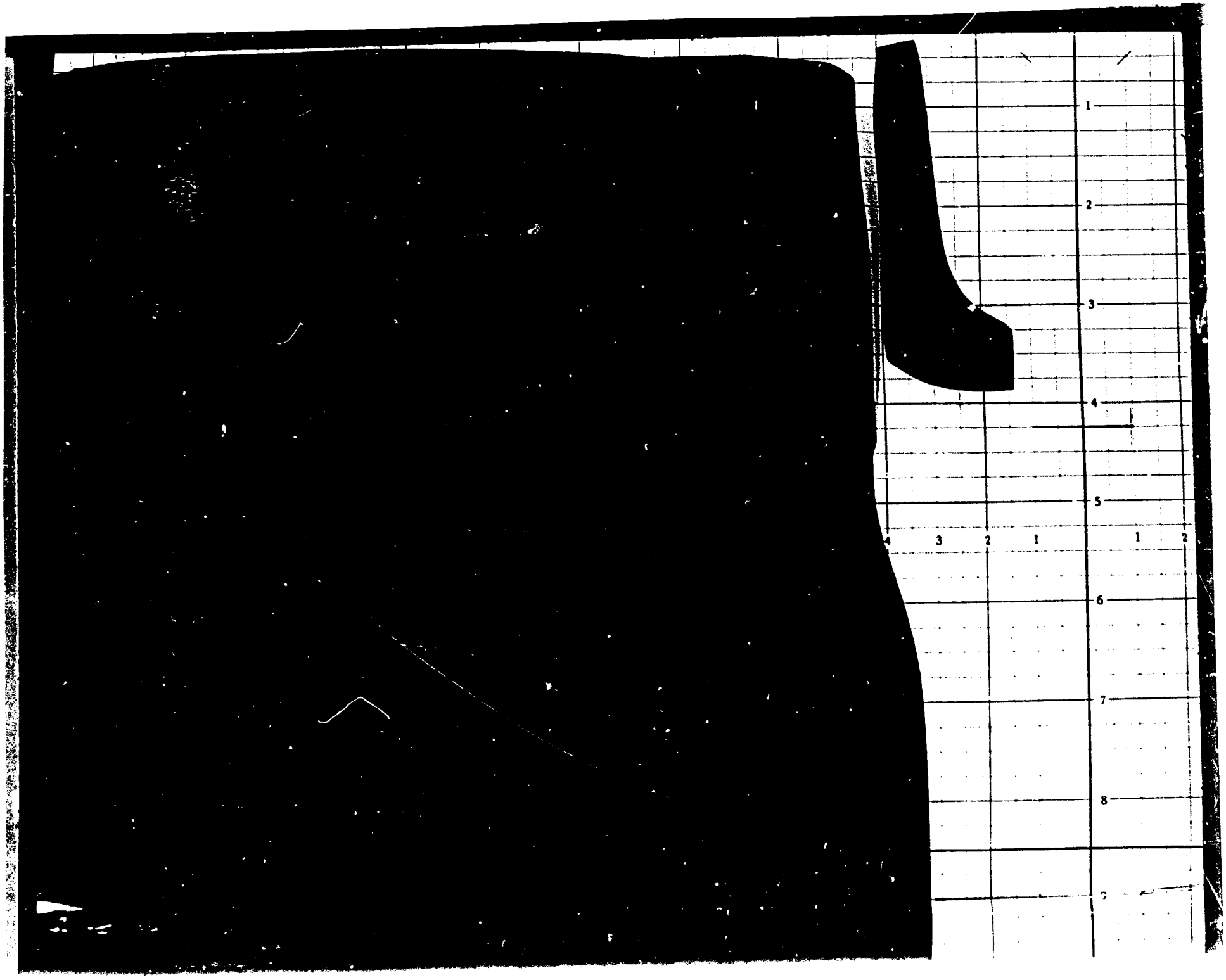
TABLE 10

ANTICIPATED PERFORMANCE OF CUSTOM LSI CIRCUIT CHIP

Maximum Sampling Speed:	3.5 MHz
Minimum Input Voltage	4 volts
With metallization for linear operation:	
Maximum output voltage swing	18 volts
Gain uniformity between channels	5%
Offset uniformity between channels	0.5 volt (nominal)
With metallization for switching mode:	
Maximum output voltage	27 volts
Rise and Fall Time Constant	10 μ seconds.

Figure 77. Preliminary LSI circuit schematic.


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-17V



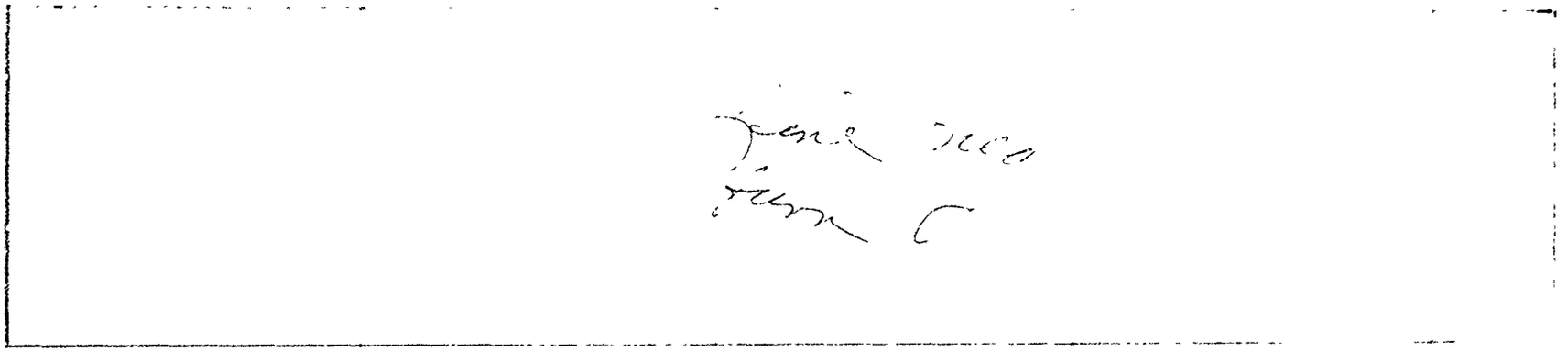
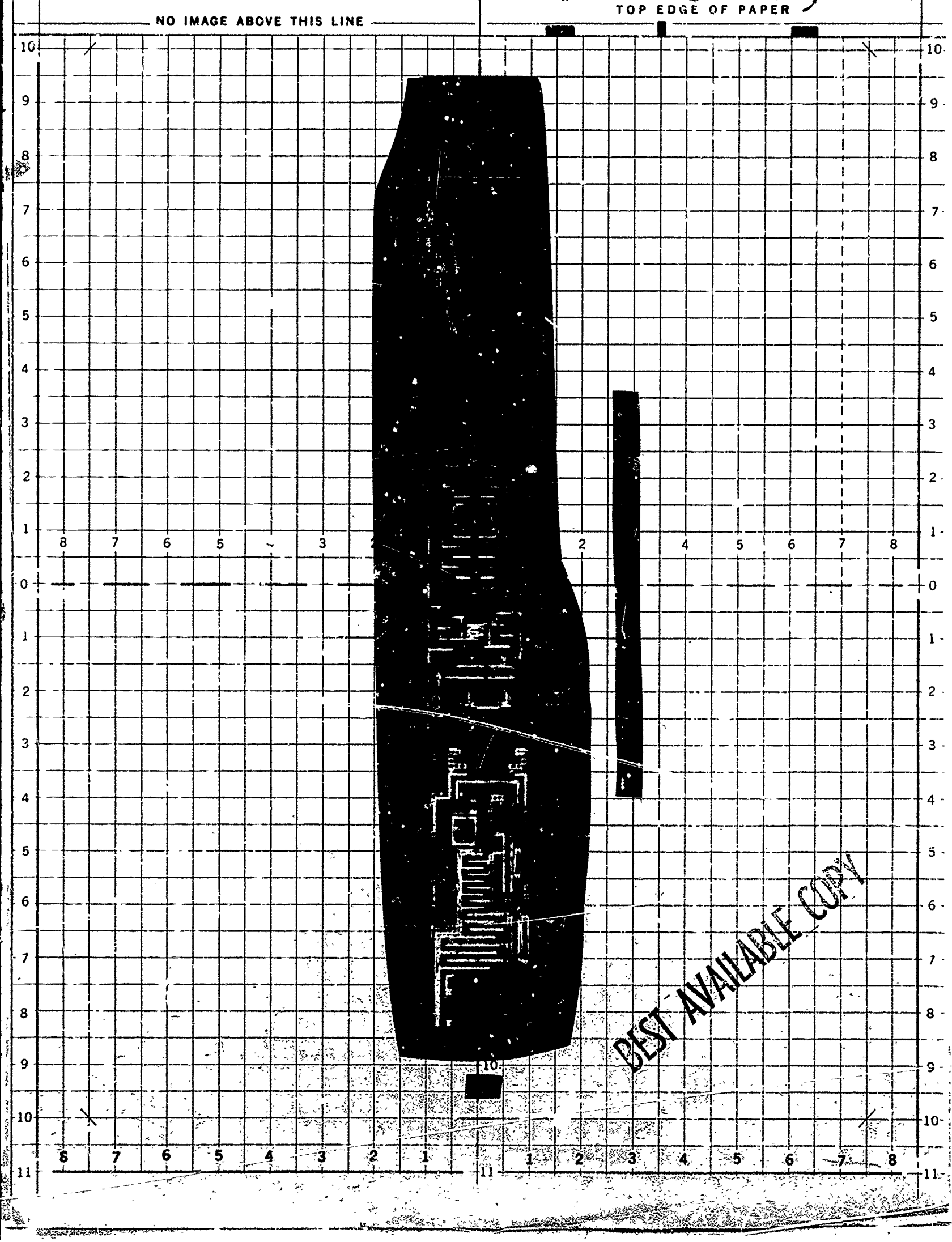


Figure 78. Preliminary LSI circuit layout.

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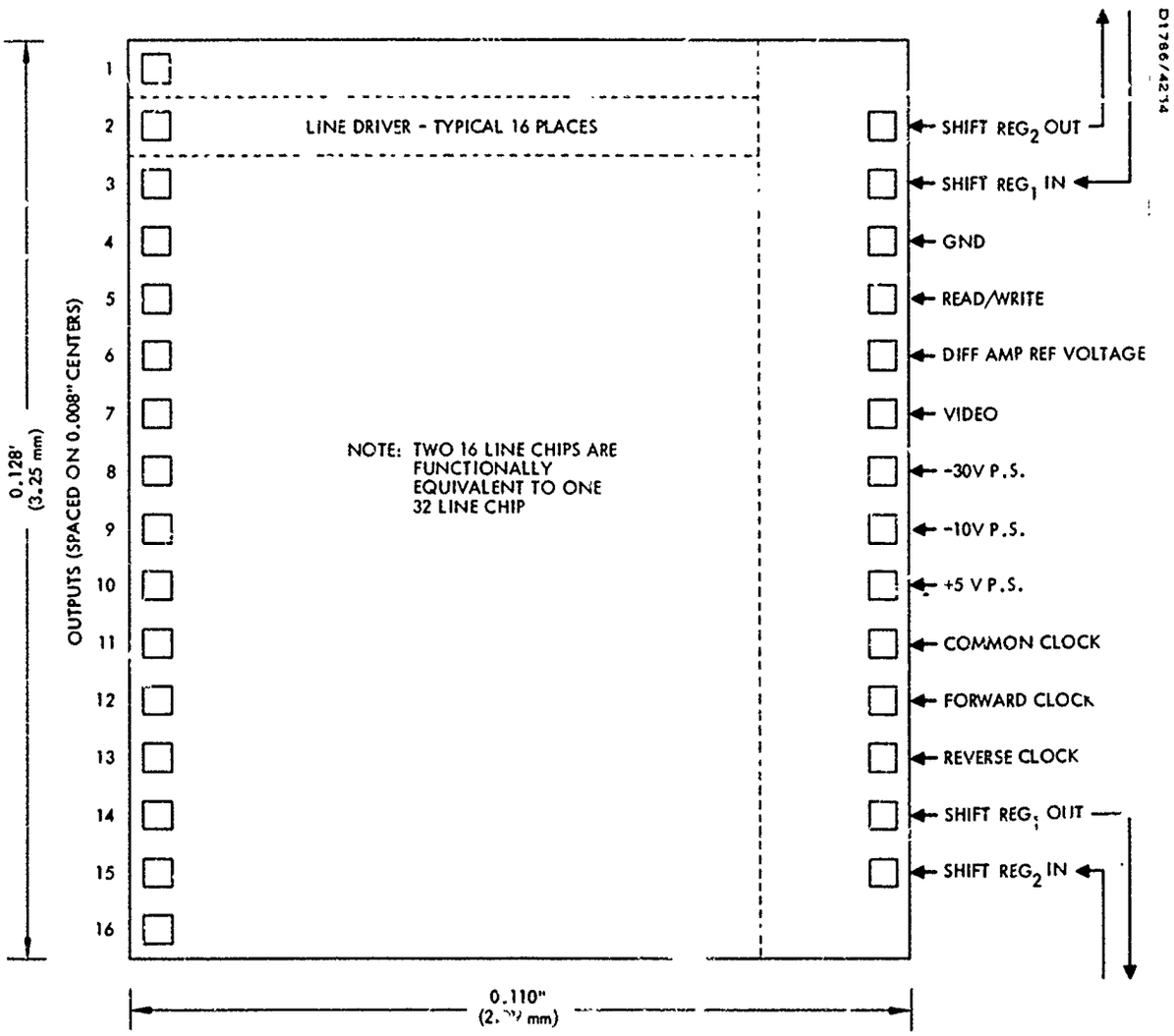


Figure 79. 16 line LSI chip layout.

the RS170 standard video must be sampled in the serial/parallel analog converter exceeded the speed capabilities of the established LSI circuit fabrication procedures except for the lowest resolution display. The required rates are shown in Table 11.

The solution traded off increased printed circuit board complexity and non-integrated circuit component count for a simpler, integrated drive circuit design. This solution calls for a simple high speed multiplexer to reduce the data rate to each drive circuit chip to approximately 3 MHz and for interweaving the outputs of the drive circuits so as to place the outputs in the correct time sampled sequence. Figures 81, 82, and 83 illustrated this approach for displays corresponding to each of the resolution categories shown in Table 11. The interweaving is shown in detail as part of Figure 83.

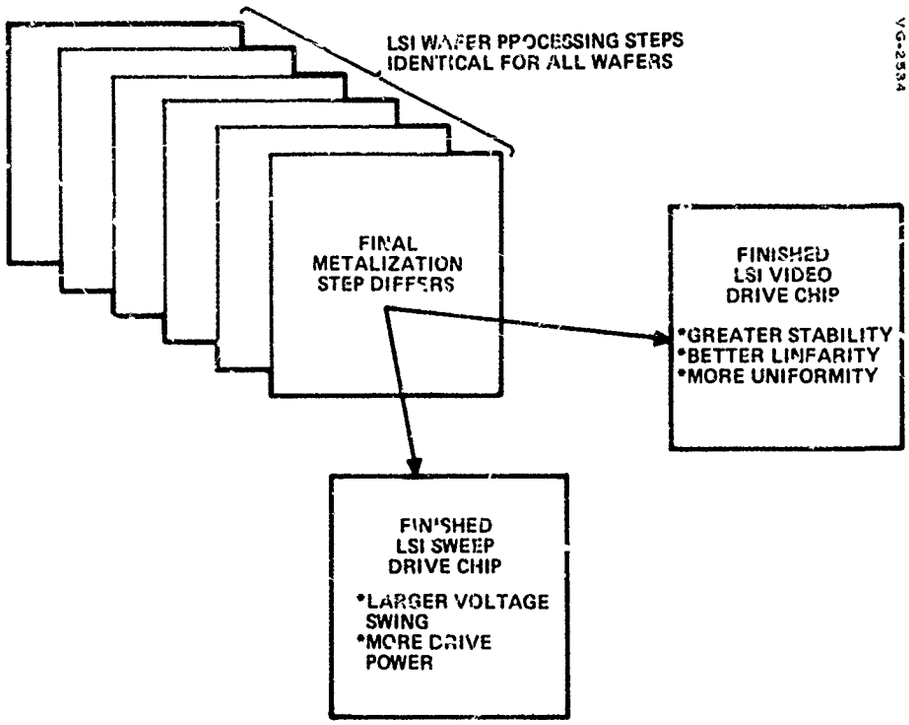


Figure 80. LSI video-sweep conversion.

CONCLUSIONS AND RECOMMENDATIONS FOR THE FUTURE

In summarizing the work done on designing a custom LSI circuit for driving a liquid crystal matrix display the following items were established: (1) Implementation of a custom LSI circuit requires no additional advances in the state-of-the-art, (2) fabrication of the drive circuits separate from the electrode-array addressing circuits (the main display chips) will lead to

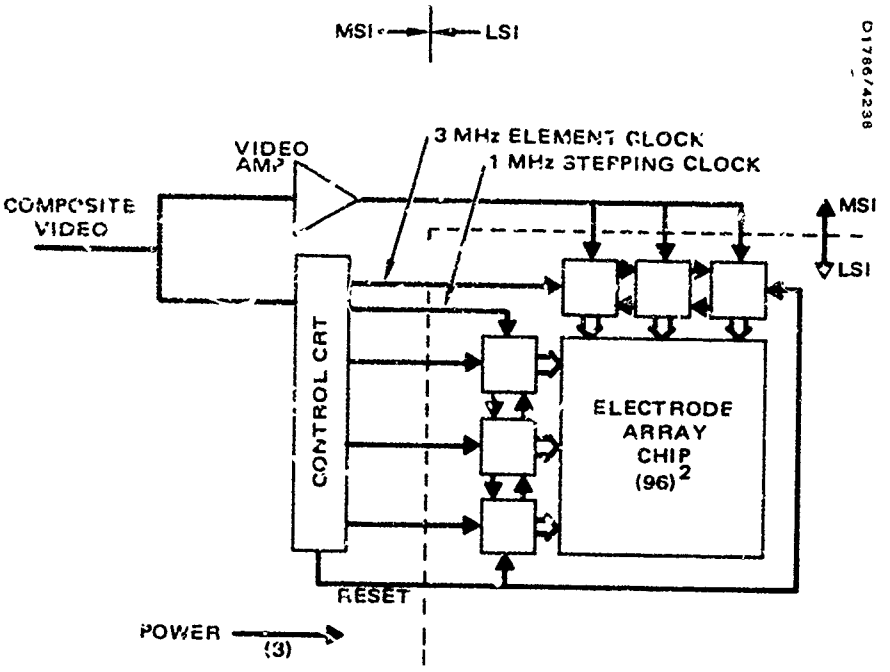
TABLE II

DRIVE CIRCUIT SAMPLING RATES AS FUNCTION OF DISPLAY RESOLUTION

Vertical resolution (lines)	Rate (MHz)
Less than $480/_4$	3.1
Less than $480/_2$	6.2
Less than 480	12.3

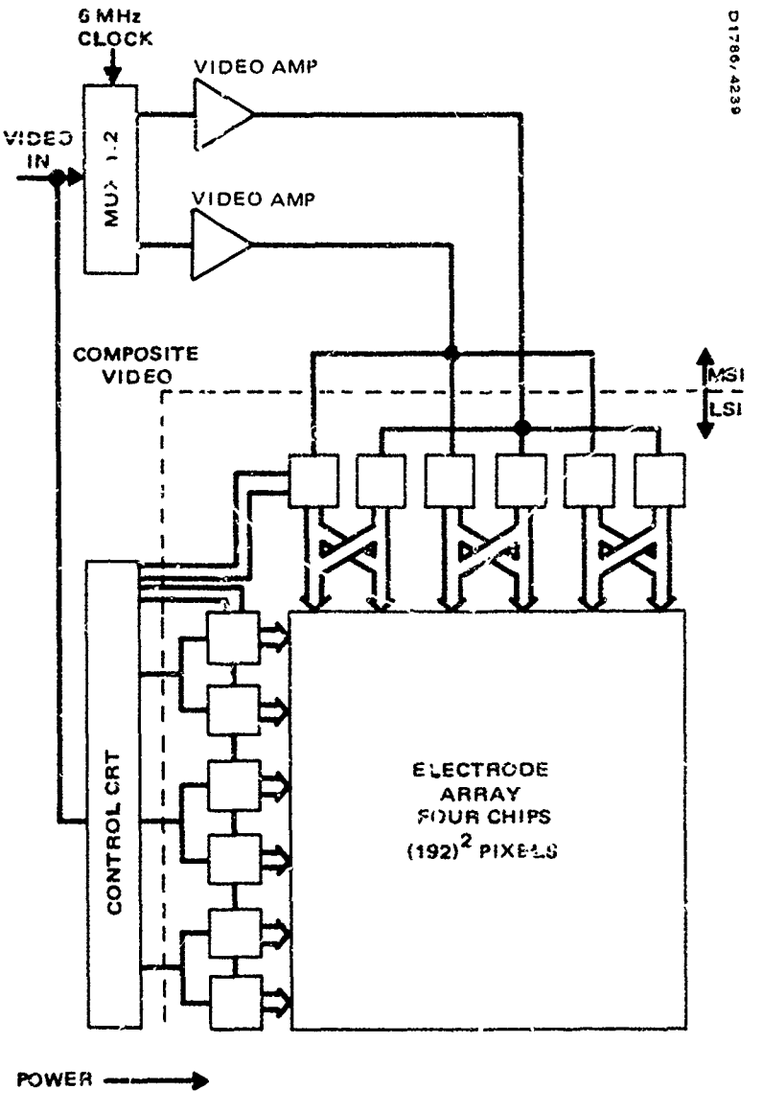
NOTE: Assumes Standard RS170,525 line television Interface and a matrix display with equal horizontal and vertical resolution density.

a higher yield of good display systems than if they were fabricated on one substrate, and (3) semiconductor circuit technology is advancing so rapidly that alternate technologies such as CCD need to be continuously evaluated for applicability.



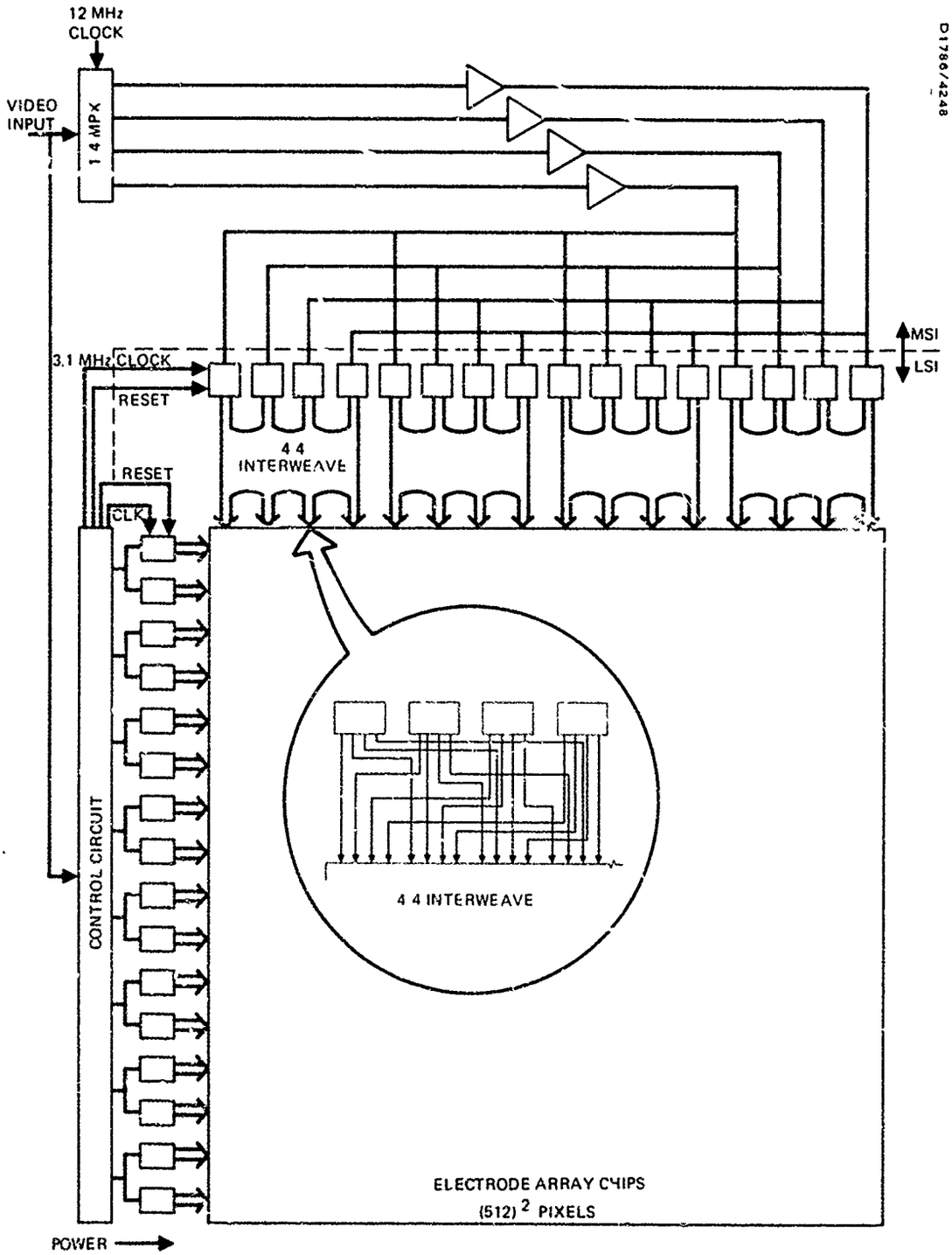
- $(96)^2$ ARRAY – ONE $(96)^2$ MODULE
- 6 x 32 LINE DRIVE CHIPS
- 7 + 3 + 1 = ~ 11 LEADS
- NO INTERWEAVING
- SAMPLING CLOCK 3.1 MHz
- FORMAT – EACH FIELD EVERY OTHER LINE UNTIL FULL
- STEPPING CLOCK – 1 MHz

Figure 81. Microminiaturized drive for single chip display.



- $(192)^2$ ARRAY, FOUR $(96)^2$ MODULES
- 12 x 32-LINE DRIVE CHIPS
- 9 + 3 + 1 = ~ 13 LEADS
- 2:2 INTERWEAVING VIDEO
- SAMPLING CLOCK 3.1 MHz
- FORMAT – EACH FIELD EVERY LINE UNTIL FULL
- STEPPING CLOCK 2 MHz

Figur 82. Microminiaturized drive for quad array display.



- $(512)^2$ ARRAY-FOUR $(256)^2$ MODULES
- 32 x 32 LINE DRIVERS
- 4 + 8 + 4 + 3 + 1 = 20 LEADS
- 4·4 INTERWEAVE
- SAMPLING CLOCK 3.1 MHz
- STEPPING CLOCK 2 MHz

Figure 83. Microminiaturized drive for TV compatible display.

SECTION VI
QUAD DISPLAY

The fabrication of a quad display requires the assembly of four electrode array chips onto a common substrate in such a manner that they form a continuous display surface with four times the active area of a single module display. To do this requires more sophisticated manufacturing and assembly techniques than those used for the single module display, and new factors are introduced which must be controlled. Among these factors are the flatness and parallelism between all four chips, the width of the gap between chips, and the alignment of the display elements on each chip with those on the adjacent chip. The degree of precision necessary to control these parameters is determined from human factors requirements regarding their effect on display performance. A brief summary of each of the important factors in the construction of the quad display will now be presented, along with a description of the associated equipment and procedures used in its fabrication.

FABRICATION PROCEDURES AND PERFORMANCE GOALS

Wafer Flatness

Since the liquid crystal display is formed by placing a thin layer of liquid crystal between the electrode array chip and a transparent glass electrode, the thickness and uniformity of the liquid crystal layer are dependent on the flatness of the array chip. It is therefore necessary to to keep the surface of the silicon wafer as flat as possible during the processing and assembly steps. It has been observed that the raw wafers obtained from the manufacturer are generally polished to a surface flatness acceptable for the display. The subsequent processing steps, however, consisting of high temperature diffusions and etching cycles, tend to introduce some degree of warping into the wafer. To remedy this effect the processing of the wafers was changed to allow the use of lower temperatures in the oxidation cycles, which consequently reduced the amount of warpage in the finished wafers.

A further increase in flatness was also gained by changing the thickness of the wafer. The standard wafers previously used for the display were on the order of 11 mils thick. While this is adequate for normal semiconductor processing, the use of thicker wafers is desirable in this particular application. The use of 19 mil wafers was therefore introduced, providing an increase of approximately 70 percent in wafer thickness and rigidity. The use of these wafers in conjunction with the lower processing temperatures provides finished electrode array chips with surface undulations of less than 0.1 mil.

Precision Sawing

The first step in the assembly of the quad display is the sawing of the individual electrode array chips. Each chip must be sawed precisely along two edges of its active area to permit it to interface closely with the adjoining chips and form a continuous display surface. A photo of such a chip is shown in Figure 84. The size of the gap between two chips must be kept to minimum to prevent it from being seen by the observer. It is therefore desired to keep the width of the gap below 1 mil (.001") to insure that it is well below the resolution of the human eye at normal viewing distance, and to minimize any discontinuity in the element to element spacing (.010") of the electrode array chips.

The sawing appratus used for this operation consists of a high speed silicon dicing saw with a diamond impregnated circular blade that rotates on air bearings at 30,000 RPM. This saw not only permits precise straight cuts to be made, but also allows for accurate angular rotations of the chip after cutting, permitting the second cut to be made at a 90^{o} angle to the first cut within an accuracy of 10 microradians.

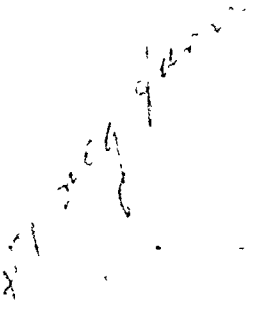
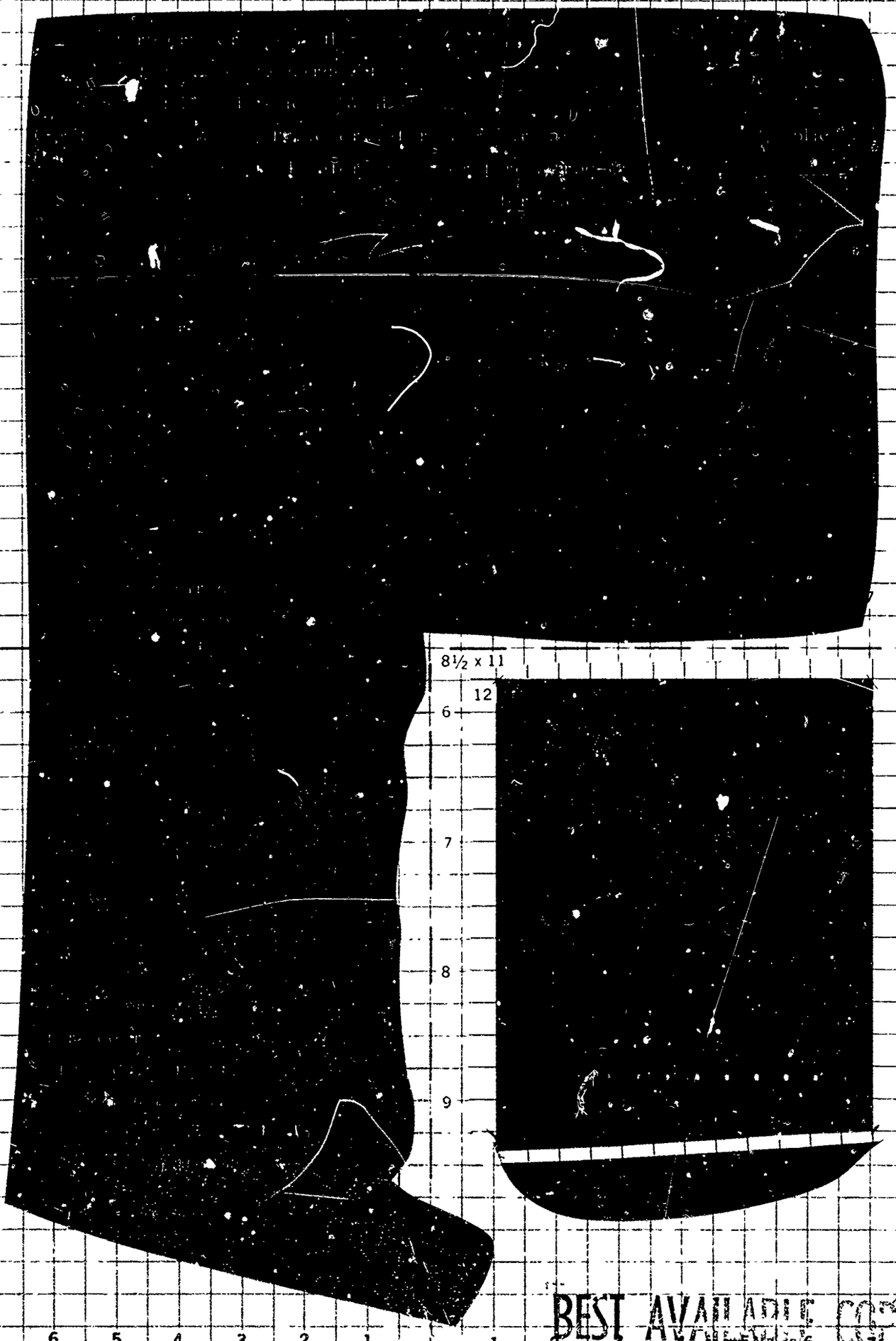


Figure 84. Sawed electrode array chip.

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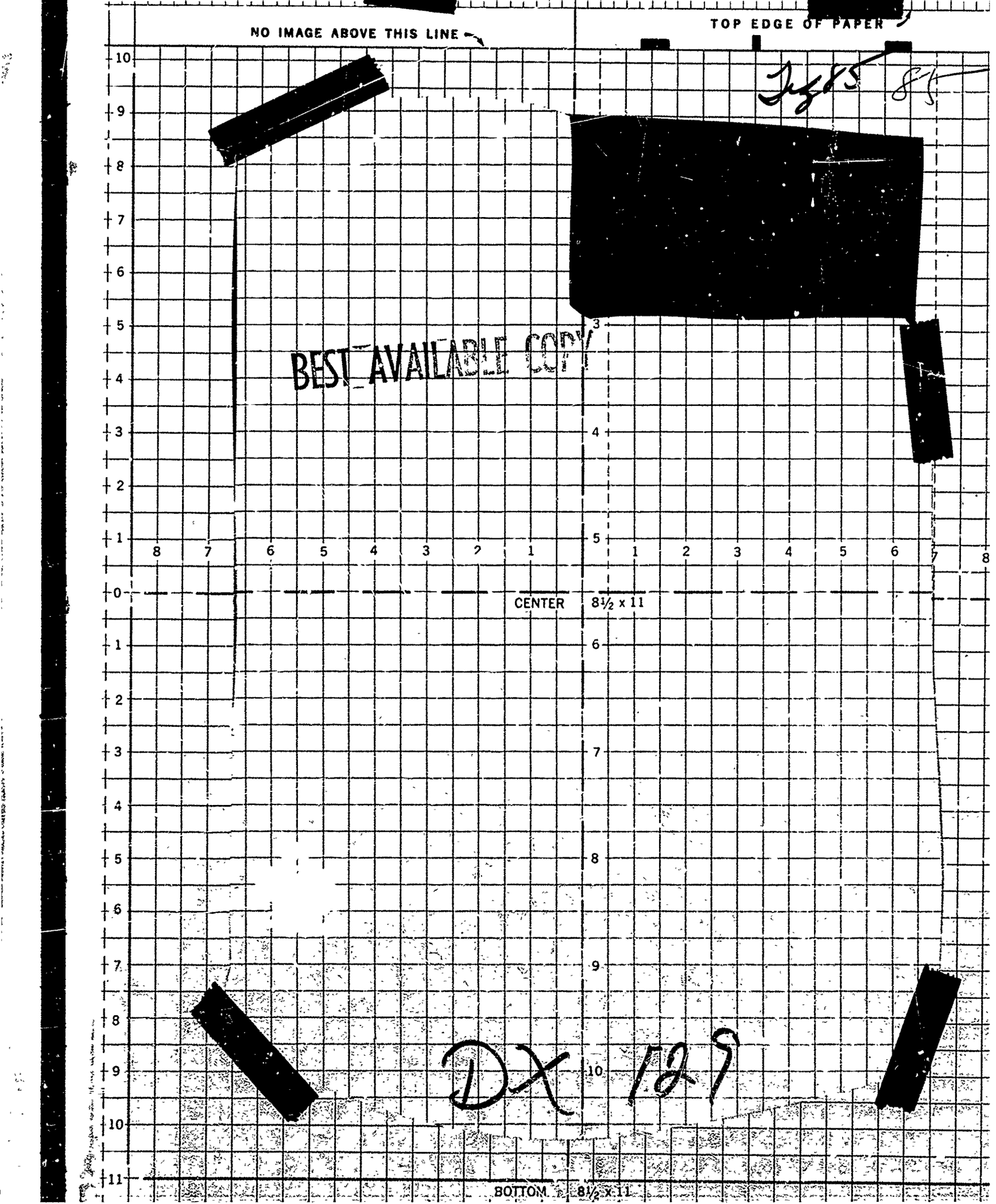
Since silicon is a hard crystalline material, the sawing action produces a certain amount of chipping on the edge of the sawed wafer. This chipping is potentially dangerous to the semiconductor electrode structure on the surface of the chip, and therefore the saw cut is made slightly outside the actual perimeter of the active area. This is shown in Figure 85. The degree of chipping that normally occurs is confined to an area approximately 0.4 mil wide, and therefore allows the saw cut to be made quite close to the active area of the chip. This spacing is less than five percent of the width of a display element, and the resulting gap width between adjacent array chips is less than 1 mil.



Figure 85. Microphotograph of module edge.

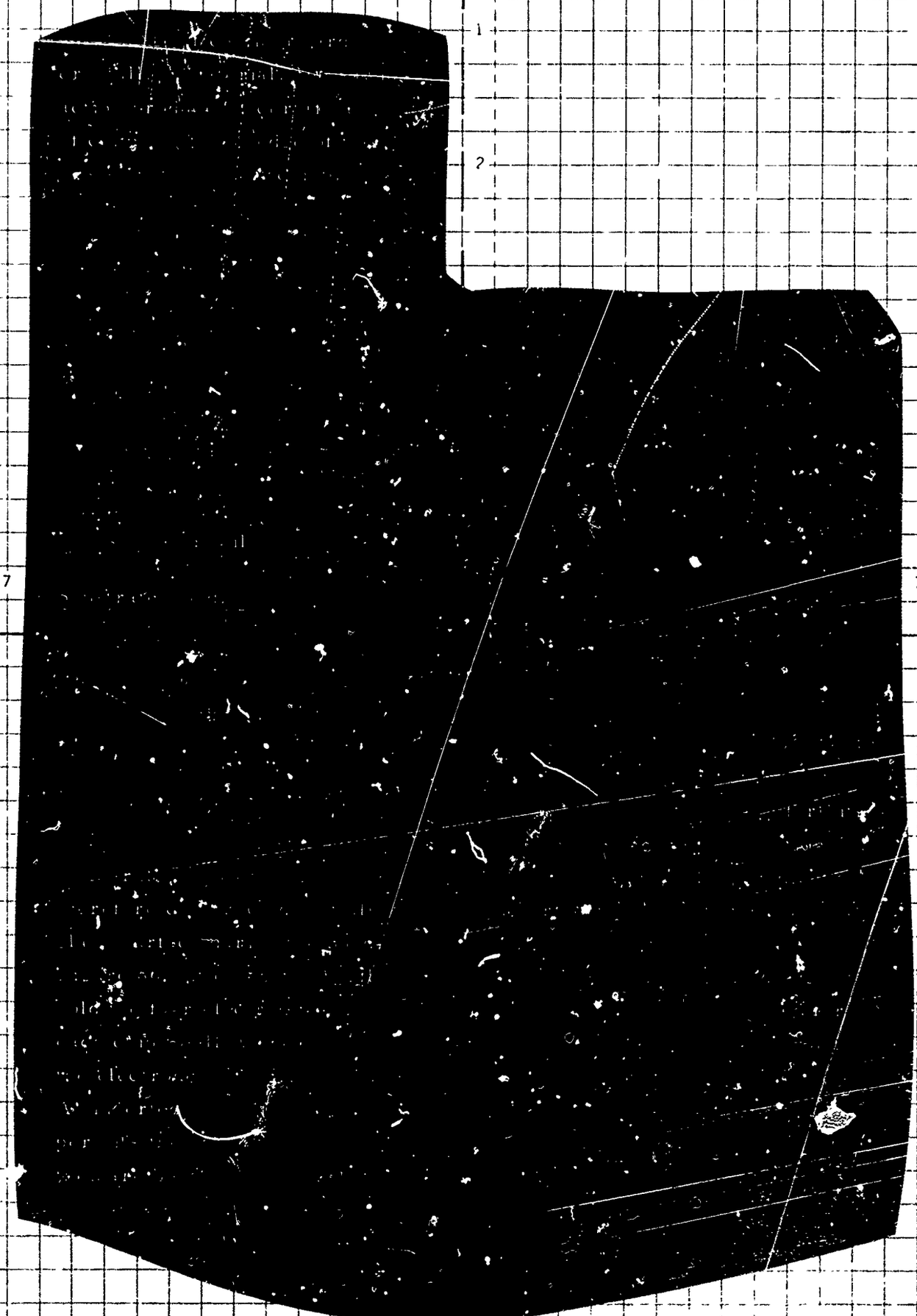
Substrate Bonding

After the electrode array chips have been sawed, they must be carefully bonded to the display substrate, which consists of a flat glass plate on which the circuit electrode lines have been etched. Since four individual chips are being used to form a common display surface, it is important not only for each surface to be flat, but the surfaces of all four chips must be coplanar as well. Slight variations in chip thickness or non-uniformities in the thickness of the bonding adhesive could lead to serious variations in the parallelism and surface heights of the chips. A special instrument was therefore constructed that allows the chip surfaces to be referenced to a flat glass surface during the bonding operation. This instrument is shown in Figure 86. It consists of a flat glass vacuum chuck specifically designed to hold the four electrode chips. A micrometer adjustment is provided for each chip to allow accurate positioning in the X and Y directions, permitting the electrodes on each chip to be aligned with those on the adjoining chip. An inverted microscope that looks through the vacuum chuck from underneath permits the operator to position the chips to the required tolerance before they are bonded to the display substrate.


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Figure 86. Inverted microscope and vacuum chuck.

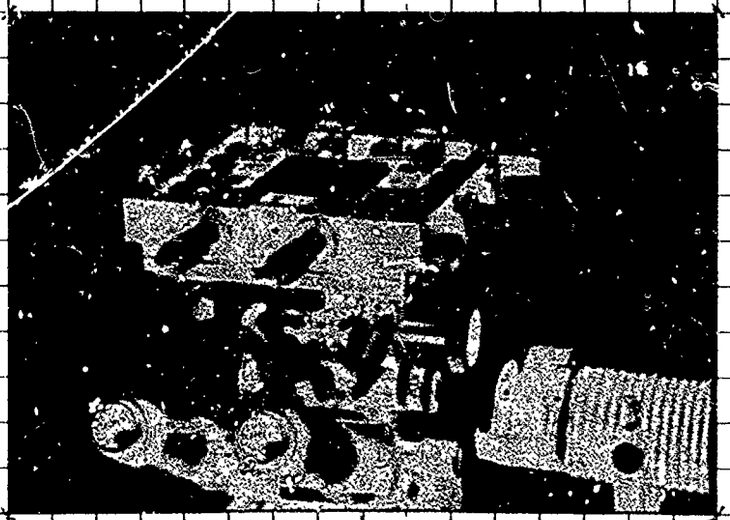
The choice of the bonding adhesive is important for maintaining flatness and alignment of the four array chips. Experience with conventional epoxy adhesives applied in their fluid state has shown a tendency for the wafers to warp as the epoxy hardens. These adhesives were therefore abandoned in favor of solid thermosetting adhesive. This adhesive consists of a thin mylar sheet that is coated on both sides with a layer of thermosetting epoxy. This material is placed over the rear surfaces of the chips on the vacuum chuck, and the display substrate is then placed on top. The entire assembly is then heated to about 125°C for several hours. The thermosetting adhesive melts and bonds the electrode array chips to the display substrate, as shown in Figure 87. In this manner the surface flatness and alignment are maintained since the chips remain in contact with the flat vacuum chuck during the bonding operation. The appearance of the display after bonding is shown in Figure 88.

Final Assembly

After the electrode array chips have been bonded to the display substrate, the display is ready for final assembly. The first step is the wire bonding of the electrode lines on the substrate plate. This is done using an ultrasonic wire bonding machine that produces reliable bonds to the 800 electrode lines. The display is then ready for filling with liquid crystal

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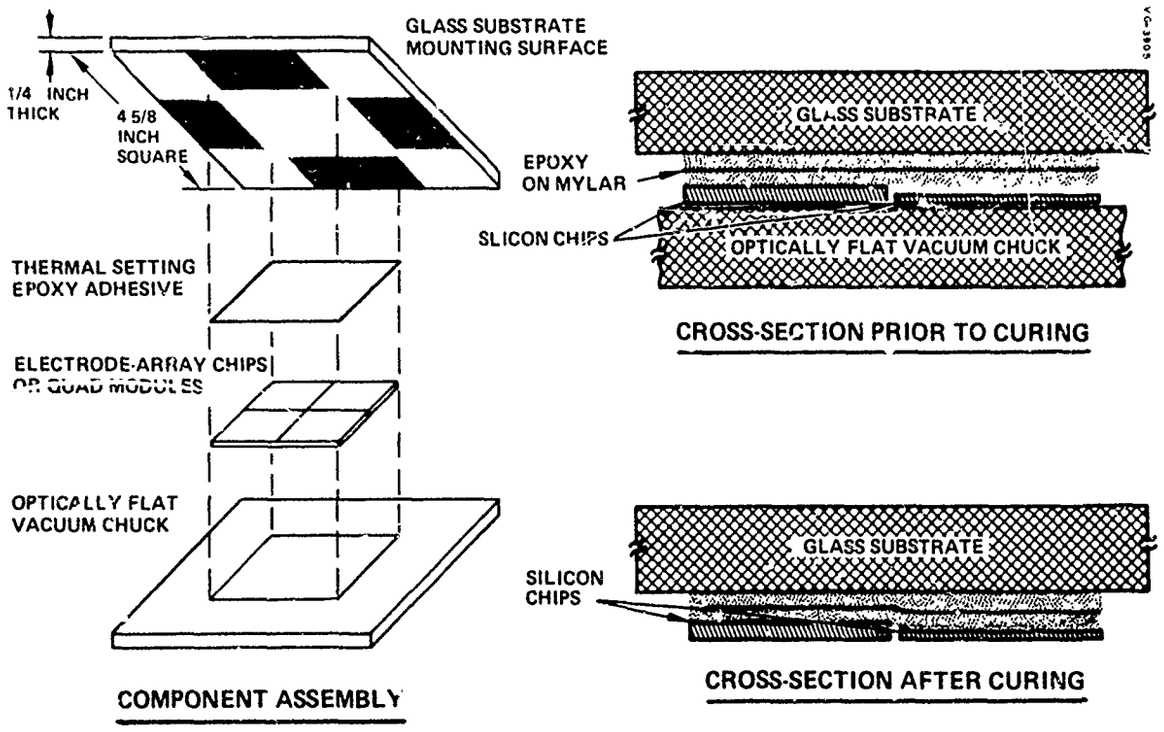


Figure 87. Quad module mounting.

material. An aluminum base frame is bonded to the display substrate outside the periphery of the array chips and wire bonds. The filling process begins by placing a small ball of indium on a special contact pad in the corners of two of the electrode chips. The balls of indium serve as contacts to the conductive coating on the surface of the counterelectrode glass. A mylar spacer is then positioned outside the active area of the display which will control the spacing between the counterelectrode and the semiconductor surface. The liquid crystal is applied along one edge of the display and the counterelectrode is lowered into place, allowing

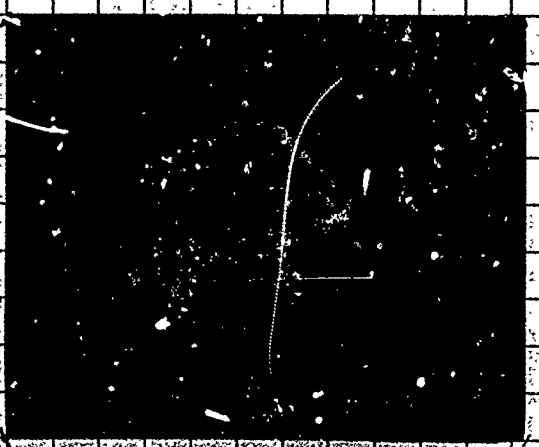
Figure 88. Quad array after mounting.

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the liquid crystal to flow across the display and fill the gap created by the mylar spacer. This completes the filling process.

To protect the liquid crystal from contamination and moisture, and provide mechanical support, a final aluminum frame is positioned over the counterelectrode glass so that it mates with the base frame bonded to the display substrate. Rubber gaskets are used between the top frame and the counterelectrode and base frame to provide a seal The top frame is held down by several screws that permit adjustment of the amount of pressure applied to the counterelectrode plate. The assembly of the quad display is now complete. A photo of the display is shown in Figure 89.

External Display Connections

Because of the large number of connections necessary to connect to the display (over 800), it was necessary to devise a special connection technique to make contact to the display while still permitting the displays to be interchangeable. Conventional connecting devices do not have the required contact density to do this job in a reasonable amount of space. The electrode line spacing on the display substrate is the same as that used on the electrode array chip - 100 per inch. A high density connector was fabricated that uses flexible KAPTON ribbon cables with etched circuit lines that mate directly with those on the display. This concept is shown in Figure 90. Alignment of the contacts on this connector is done visually, with an elastomer pressure pad supplying the contact force. The opposite ends of the lines on the KAPTON ribbon cable are terminated in standard ribbon cable connectors that interface with the external drive electronics unit. An overall view of the finished connector is shown in Figure 91. It allows the displays to be easily interchanged and can itself be disconnected from the drive electronics and interchanged.

Figure 89. Completed quad display.

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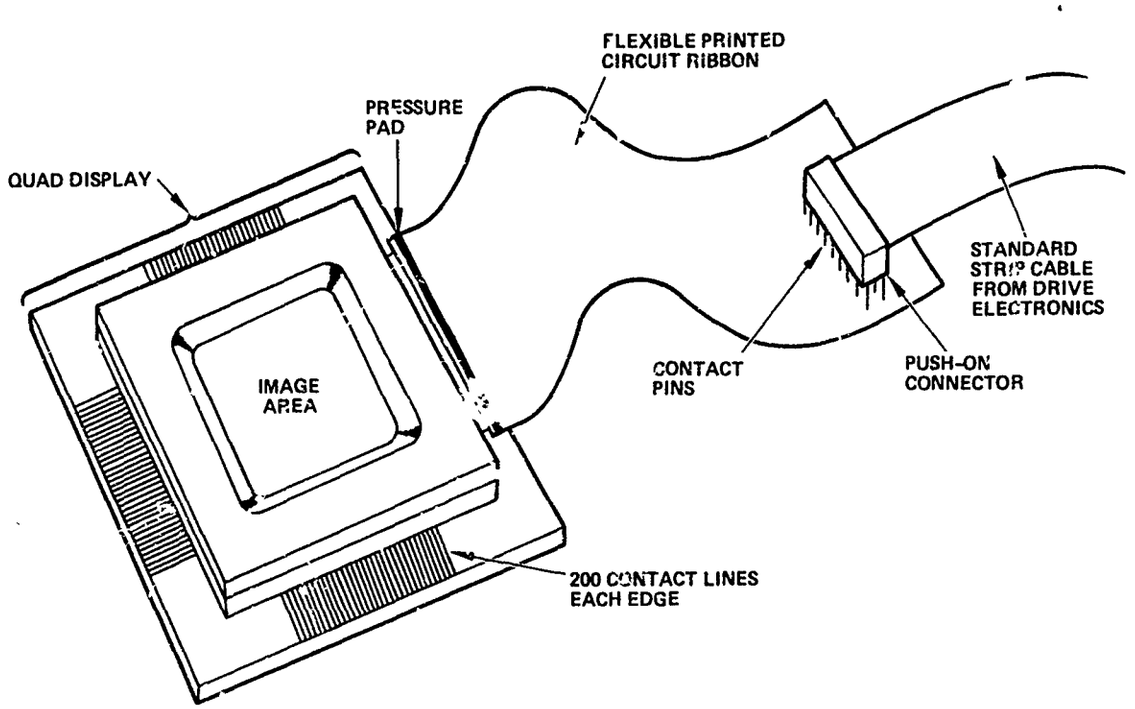


Figure 90. High density connector concept.

QUAD PERFORMANCE

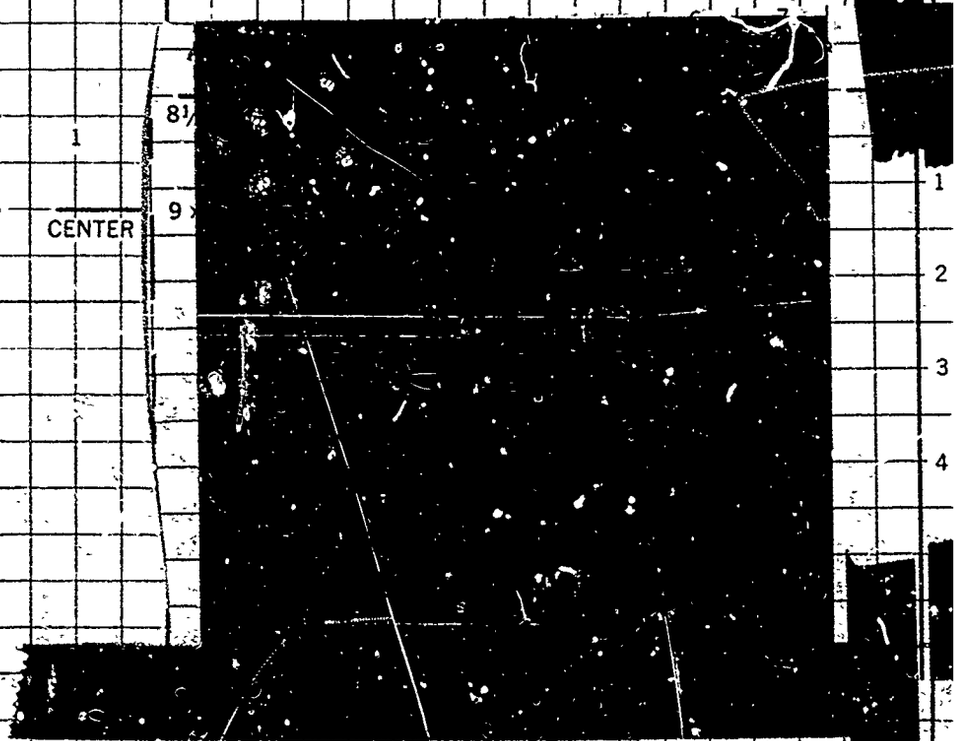
The effectiveness of the manufacturing techniques mentioned in the previous section was tested with the construction of four quad displays. The fabrication of the first three displays was primarily intended to provide information and experience in the various manufacturing operations. The fourth display was the product of this experience and served as a model for evaluation of the performance that can be expected from the modular construction techniques developed thus far.

Figure 91. Quad connector assembly.

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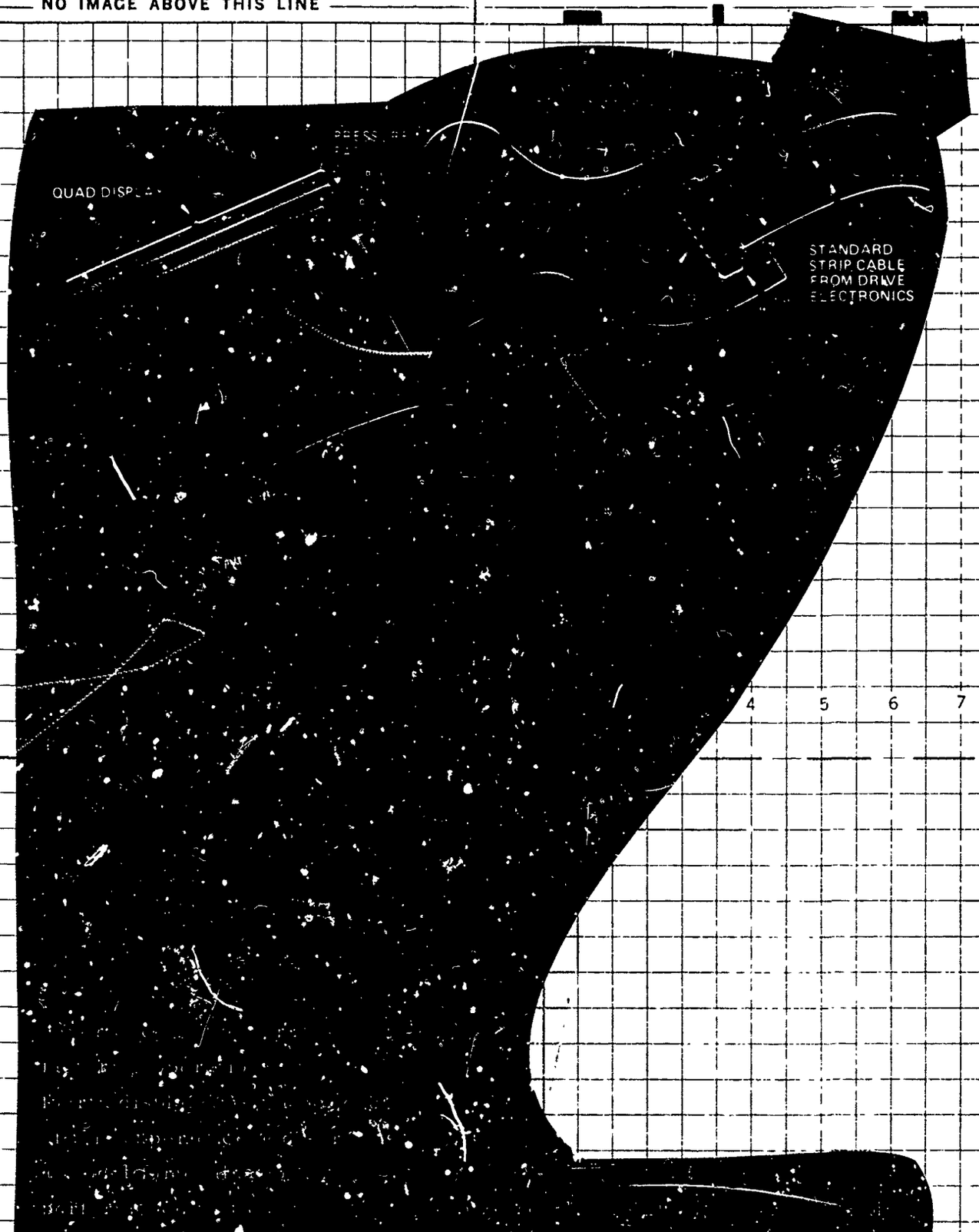
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The performance of the quad display was measured in terms of normal display parameters such as brightness, contrast, surface defects, and uniformity. Those factors introduced due to the moduiar construction of the display, such as flatness variations and gaps between chips, had to be studied to determine their effect on display quality. These parameters can normally be measured by direct observation of the display surface under a microscope.

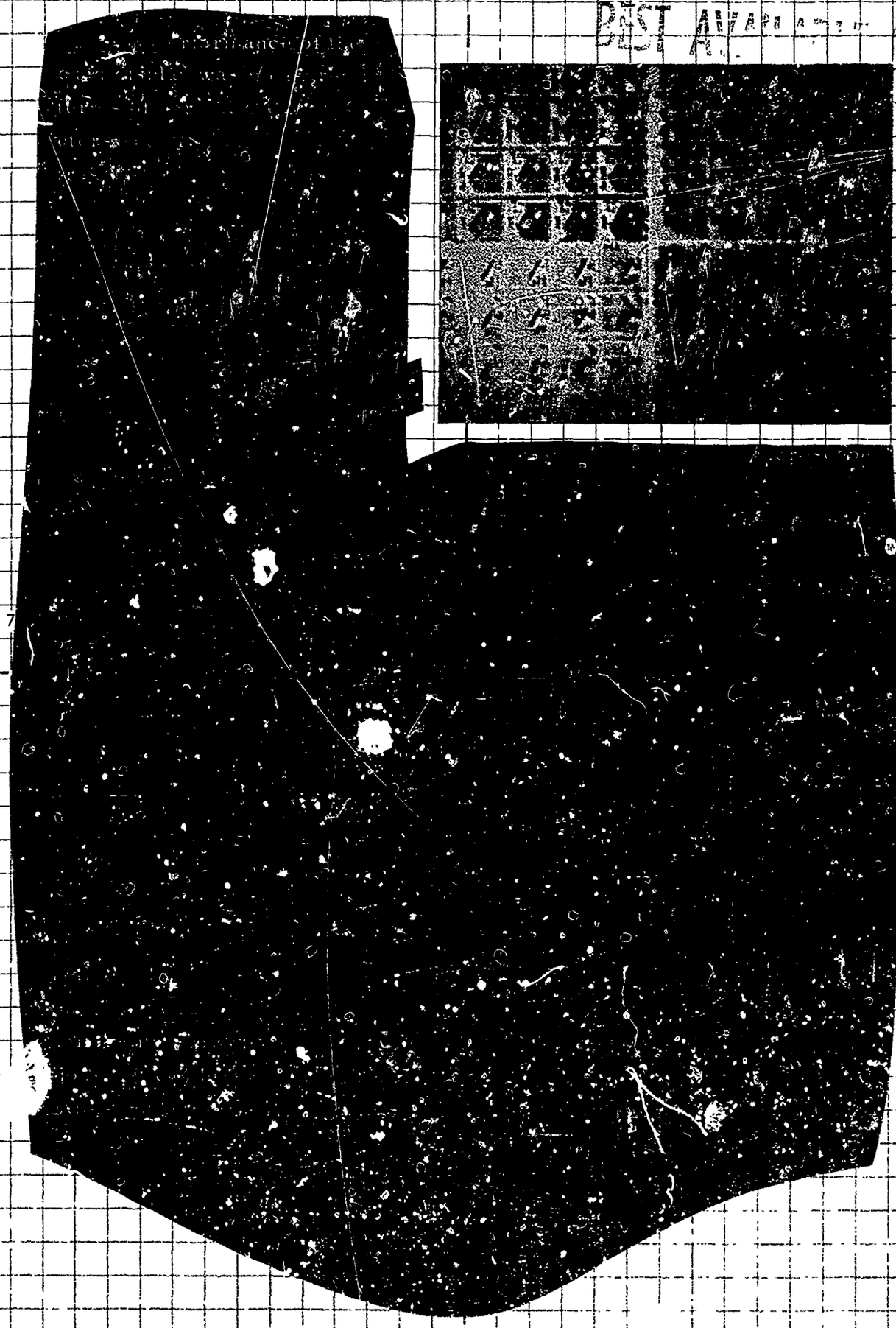
Figure 92. View through microscope.

The size of the gap between chips can be seen in Figure 92. This is a magnified view of the four chip intersection at the center of a typical quad display. Using the 10 mil spacing between elements as a reference, it can be seen that the width of the gap is less than 1 mil and the alignment between electrode structures is on the order of 0.5 mil.

Photos of each of the quad displays that were built have been shown previously in Figure 14. It can be seen that the first three displays contain a large number of line defects, or even entire chips that are non-functioning. These displays were tests of the sawing and bonding accuracies, and were intended to show whether the gap between chips is visible. It is apparent from these photos that the gap is visible, even though its width is less than the performance goal. This is primarily due to the fact that most of the surface defects and non-uniformities begin and end at the edges of the individual chips. This accentuates the junction between the chips and makes the gap seem visible. It is therefore as important to control the surface uniformity and defects as it is to control the accuracy of the chip intersections. It can be seen from the photo of Quad No. IV that the position of the gap is not immediately apparent if no defects are present, even though this

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display still possessed slight non-uniformities in brightness between the four chips.

The chips used in Quad No. IV originally had no line defects. These defects were introduced during the sawing operation and are caused by electrode lines that shorted to the silicon substrate. Most of these defects are concentrated on the upper right hand chip, which was a substitute chip from a different production lot used to replace the original chip, which was broken. It is possible that process variations in that production lot were responsible for this chip's susceptibility to damage during sawing.

The brightness and contrast of this display were measured under a typical viewing arrangement for an aircraft panel installation. The display was placed in front of a photometer located at the observer position. The display was tilted back at a 30° angle with respect to the observer, with a light trap blocking the specular reflection. Light sources were located at angles of 18° azimuth and 23° elevation measured from the display normal. These positions permit the observer to view the display over $\pm 15^{\circ}$ viewing window in azimuth and $\pm 5^{\circ}$ in elevation. Under these conditions the brightness of the display, expressed as a percentage of the brightness of a perfect diffuser, ranged between 40 percent and 85 percent within the viewing window. The contrast ratio ranged between 8/1 and 13/1 within the same window. This allows the presentation of at least five shades of gray, independent of the intensity of the incident illumination.

SECTION VII
MULTIMODULE ARRAY ASSEMBLY

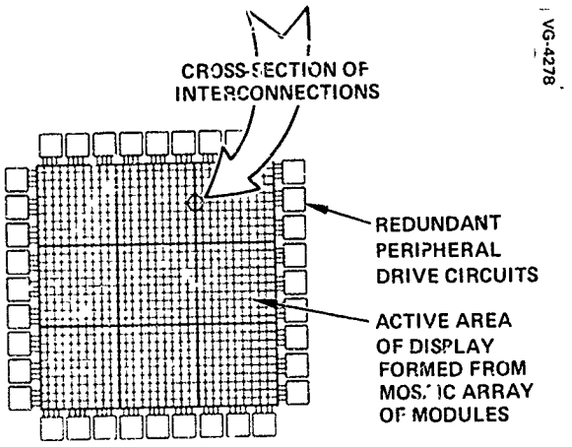
INTRODUCTION

At the present time, the largest operating liquid crystal pictorial display is a two-inch by two-inch display formed by assembling four one-inch by one-inch chips in a quad array. The development of still larger displays requires either larger chips or larger mosaic arrays of chips. Significantly larger chips are presently unavailable at a reasonable cost because their use is too limited to justify the very large tooling costs required to bring down the unit production costs. Large mosaic arrays of chips have not been assembled because there has been no way to make electrical connection to the interior chips, i.e., those chips that are completely surrounded by other chips. The quad geometry is the largest array that permits the use of only peripheral electrical connections.

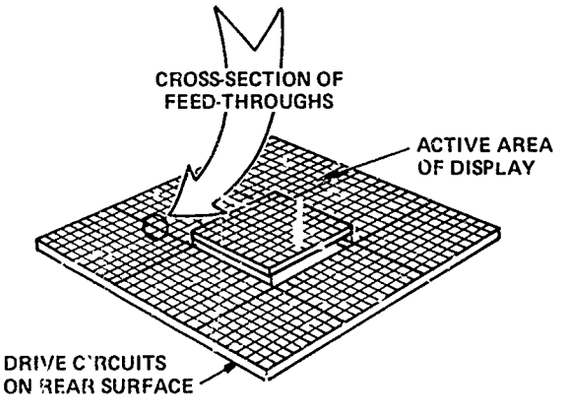
Although the general trend in the semiconductor circuits industry is towards larger and larger wafers and chips, the trend is too gradual to warrant postponing development of larger displays until the larger wafers become economically feasible. Therefore, several techniques for forming large displays by assembling an array of smaller chips have been investigated. These techniques can be separated into two basic approached — electrically interconnected modules and self-contained modules.

In the interconnected approach, as shown in Figure 93a, the drive circuits are placed around the periphery of the display and electrical connection must be made across each module-to-module junction. An interior module is thus driven with electrical signals that are fed from the peripheral drive circuits across the row and column electrode busses of the individual modules and across their interconnected junctions at the module interfaces.

In the self-contained concept, the drive circuits are placed behind each display module as shown in Figure 93b. Electrical connections are made to the individual modules from the rear by some type of front-to-back conduction scheme Since each module and its drive circuitry are self-contained, the total array size possible is essentially unlimited.



a. Interconnected modules



b. Self-contained modules

Figure 93. Basic approaches to constructing mosaic arrays.

The various techniques considered for implementing the interconnected and self-contained module approaches are presented in the next two sections. Primary emphasis was placed on finding techniques usable with the present basic MOS FET module structure, although others were considered. Fabrication methods and processing sequences are identified and described, and the tradeoffs conducted to determine the most feasible method of constructing a mosaic array of display modules are contained in the next two sections. The final section presents the conclusions and recommendations of these mosaic array assembly techniques.

INTERCONNECTED MODULE APPROACH

The most useful configuration for the interconnected module approach has the drive circuits positioned around the display periphery as shown in Figure 93a. This configuration is preferred because if a drive circuit on one side fails, the drive circuit on the other side ensures continued operation. Likewise, any break in an electrode bus on an interconnection between modules does not produce an inactive line on the display since each line is driven from both sides.

In this interconnected module approach, the electrode busses used to X-Y address each element are brought out to the periphery of each module, and the electrical continuity of each row and column electrode bus is established across the module-to-module junction. The two basic interconnect techniques are: (1) to form conductive bridges directly between module faces; and (2) to bring the electrode bus connections to the back of the module and then connect from module to module using printed circuits on a separate mounting plate. The latter technique can be accomplished several ways, however, they all require some means for making contact to the mounting plate

Bridging Technique

The bridging technique uses thin conductive bridges, as illustrated in Figure 94, to provide electrical connection between the corresponding electrode busses along each module's upper surface. It uses fabrication procedures that are similar to the well established techniques used to build storage tubes. However, the increased number of processing steps required leads to increased chances for errors, and an error in any one step means starting over again, unless some repair capability can be devised.

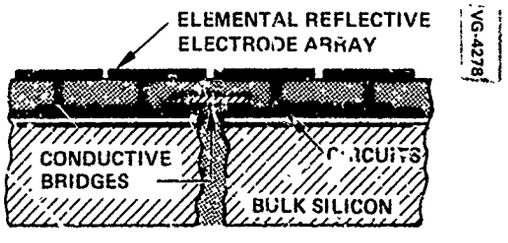


Figure 94. Bridging technique for interconnecting modules.

Wrap-Around Conductors

In addition to the bridging technique, module-to-module interconnection can also be made by bringing the connection down the side of one module, across, and up the side of the adjacent module. Conductive fingers are formed around the edge of the silicon chip at the location of each row and column electrode bus in the manner shown in Figure 95. Thus, a 100 by 100 pixel module would have 400 wrap-around conductors along the chip periphery. Contact bumps to provide electrical contact between the modules can be placed either on the side of the modules, as in Figure 96a, or on the back of the modules, as in Figure 96b.

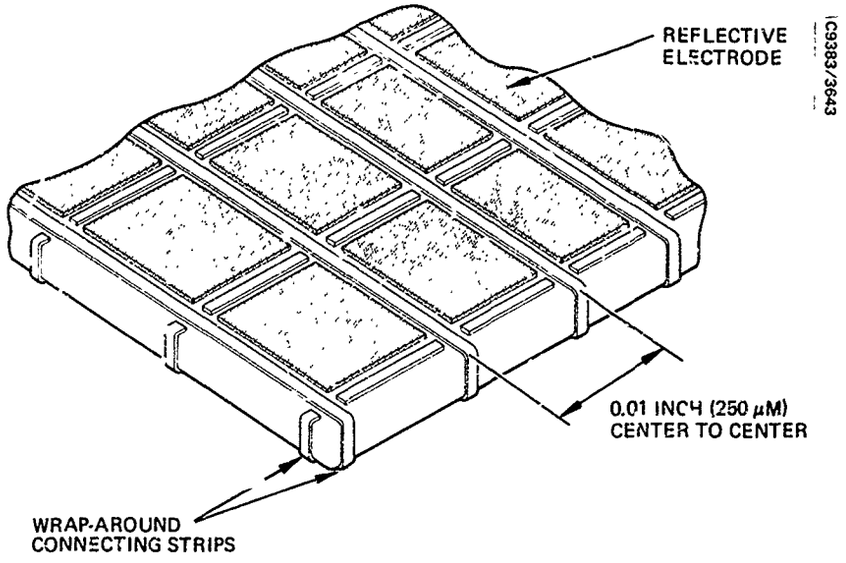


Figure 95. Wrap-around conductor approach for interconnecting modules.

In the case of contact bumps on the rear, the connection between modules is actually made on an underlying printed circuit board. This board contains conductive strips in the X and Y directions, as shown in Figure 97a, which mate with the conductive bumps to electrically connect adjacent modules. Alternatively, a double layer printed circuit board can be used, as shown in Figure 97b. The conductive strips in the X-axis can be placed on one layer and connected, and the strips in the Y-axis placed on a second layer and connected. When the display modules are appropriately placed such that the wrap-around conductors on the rear of the modules make contact with the X and Y conductive strips on the double-layer circuit board, all X-electrode busses are

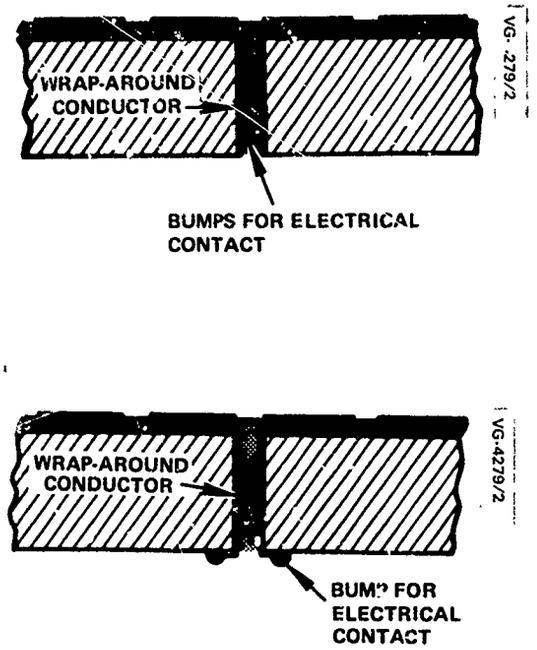
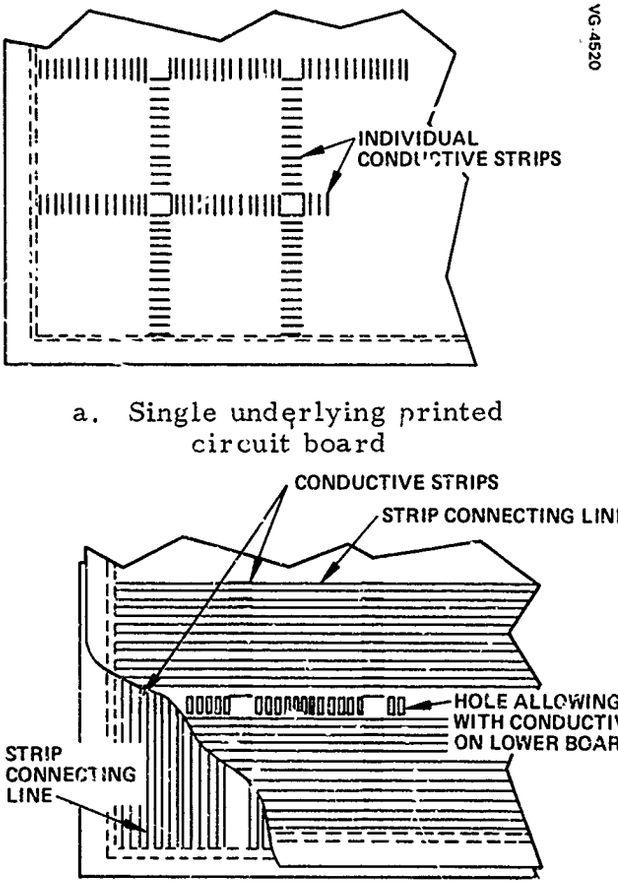


Figure 96. Wrap-around conductors for interconnecting modules.

electrically interconnected, and all Y-electrode busses are electrically interconnected. This technique is particularly advantageous because the probability of a line being out due to an open circuit is greatly reduced. For even a portion of a line to be out, there must be no less than two open circuits on the same line of the same module.

No printed circuit board is required for electrical contact using the side bumps. Instead, after the wrap-around conductors are formed, a bump is placed at each X and Y electrode position on the side of the module, for example by placing the edge of the module in a plating solution, and plating the wrap-around conductors along the side with indium. By aligning the bumps and pressing two adjacent modules together, electrical module-to-module interconnection is accomplished. The alignment process, however, would be extremely difficult with indium bumps since the chips cannot be slid laterally or separated once they have been meshed.



a. Single underlying printed circuit board

b. Double layer printed circuit board

Figure 97. Mounting board for interconnected module with wrap-around conductors

Conductor-Coated Holes

Another method of making electrical contact from the display surface side of the module to the rear surface is the use of a series of laser-drilled, conductor-coated holes as shown in Figure 98. Laser drilled holes have been formed in Indium-Antimony 0.011-inch thick (see Figure 99), and the process should be extendable for use with silicon.

With the conductor-coated hole technique, a hole would be required at the position of each column and row electrode bus along the module perimeter. Thus, a 100 by 100 pixel module would require 400 laser-drilled holes and metal contact bumps. The latter are to provide the electrical contact between the conductor coated holes and conductive strips on a printed circuit board such as that shown in Figure 97. The double layer configuration of Figure 97b is preferable to the single layer configuration of Figure 97a for the same reasons as before; that is, since all the X and Y conductors in any line are redundantly connected, it becomes far less likely that an open circuit will result in an inactive line.

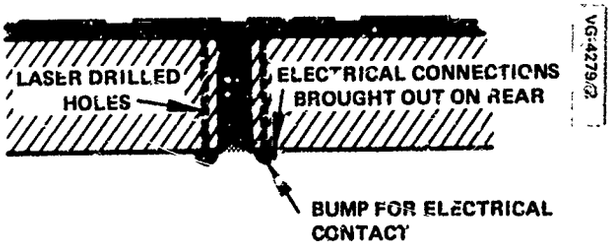


Figure 98. Conductor-coated hole technique for interconnecting modules.

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a. Top view (200X)

3 1/2 x 2 1/2

b. Cross section (160X)

Figure 99. Laser drilled holes in InSb.

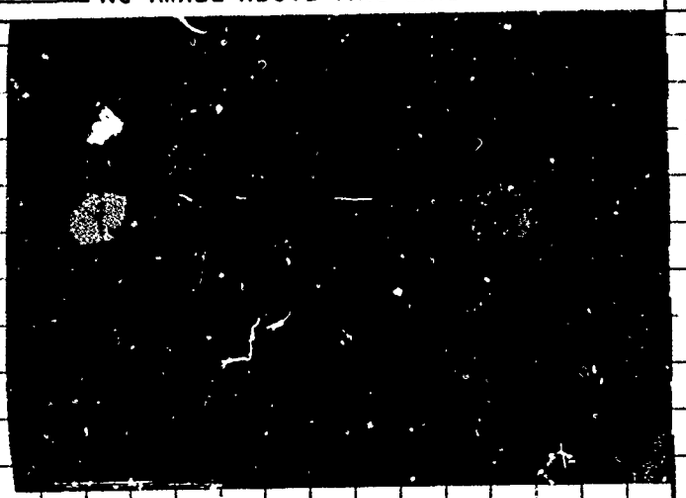
SELF-CONTAINED MODULE APPROACH

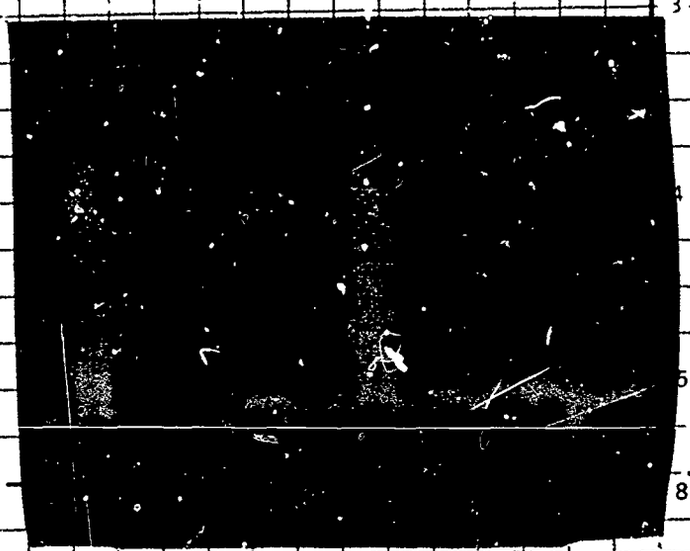
In the self-contained module approach, the display drive circuits are placed at the rear of each module and electrical connections are made to the front surface. Although the drive circuits could be positioned on the rear surface of the silicon chip, it will be simpler to fabricate then on a ceramic substrate using hybrid technology and then electrically connect them to the rear of the module. The self-contained approach has the advantage of great flexibility, since the size of the display can be altered by simply changing the number of modules being used. Also, a defective module can potentially be replaced and the display panel resealed.

Four techniques are considered for use in the self-contained module concept. The first two, wrap-around conductors and conductor-coated holes, have been previously discussed in connection with the interconnected approach

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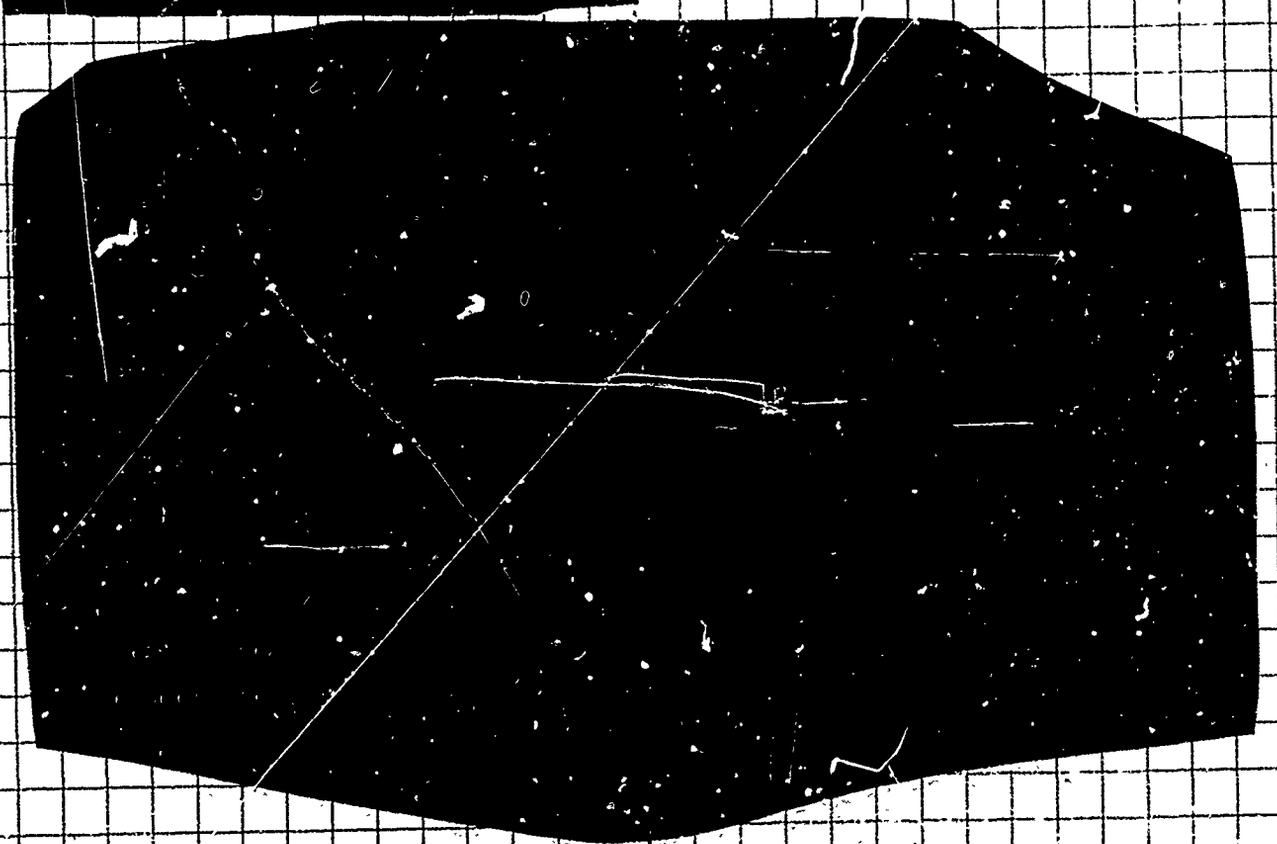
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(i.e., peripheral drive). In the self-contained module configuration, the wrap-around conductors or conductor coated holes are used to electrically connect the row and column electrode busses of the addressing circuits or the top surface of the chip to the drive circuits on a ceramic substrate at the rear of the chip. In the other two techniques, the addressing circuits are placed on the rear surface of the silicon chip and each connection to an elemental reflective electrode in the display matrix is brought through the silicon chip thickness. These "through the silicon" methods are the transistor feed-through and the deep-etched hole. Since the addressing circuits are on the back of the chip in each case, connection to the hybrid drive circuit package can easily be made using indium bump contacts, or a related technology. Connection of the drive circuits to the control electronics can be made by means of 8 to 16 wires from each module to a printed circuit board.

Wrap-Around Conductor

In the self-contained module approach, the wrap-around conductors provide an electrical connection between the X and Y electrode busses on the top surface of the module and the drive circuits at the rear. This technique is analogous to that used in the interconnected approach, and is illustrated in Figure 100. The self-contained modules can be assembled into a mosaic array, as shown in Figure 101.

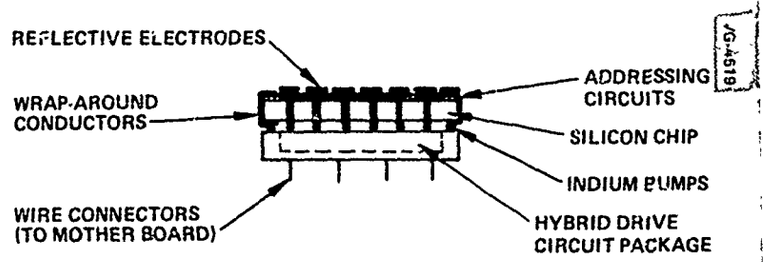


Figure 100. Wrap-around conductor technique for self-contained module (side view after assembly).

Conductor-Coated Holes

In the self-contained module approach, the connection between the addressing circuits on the display surface of the silicon chip and the drive circuits at the rear can be made by means of laser-drilled, conductor-coated holes. Electrical connection is made to the holes at the top and bottom surfaces of the silicon chip as illustrated in Figure 102. Connection at the front surface is made to the polysilicon electrode bus lines which run horizontally and vertically directly under the front surface

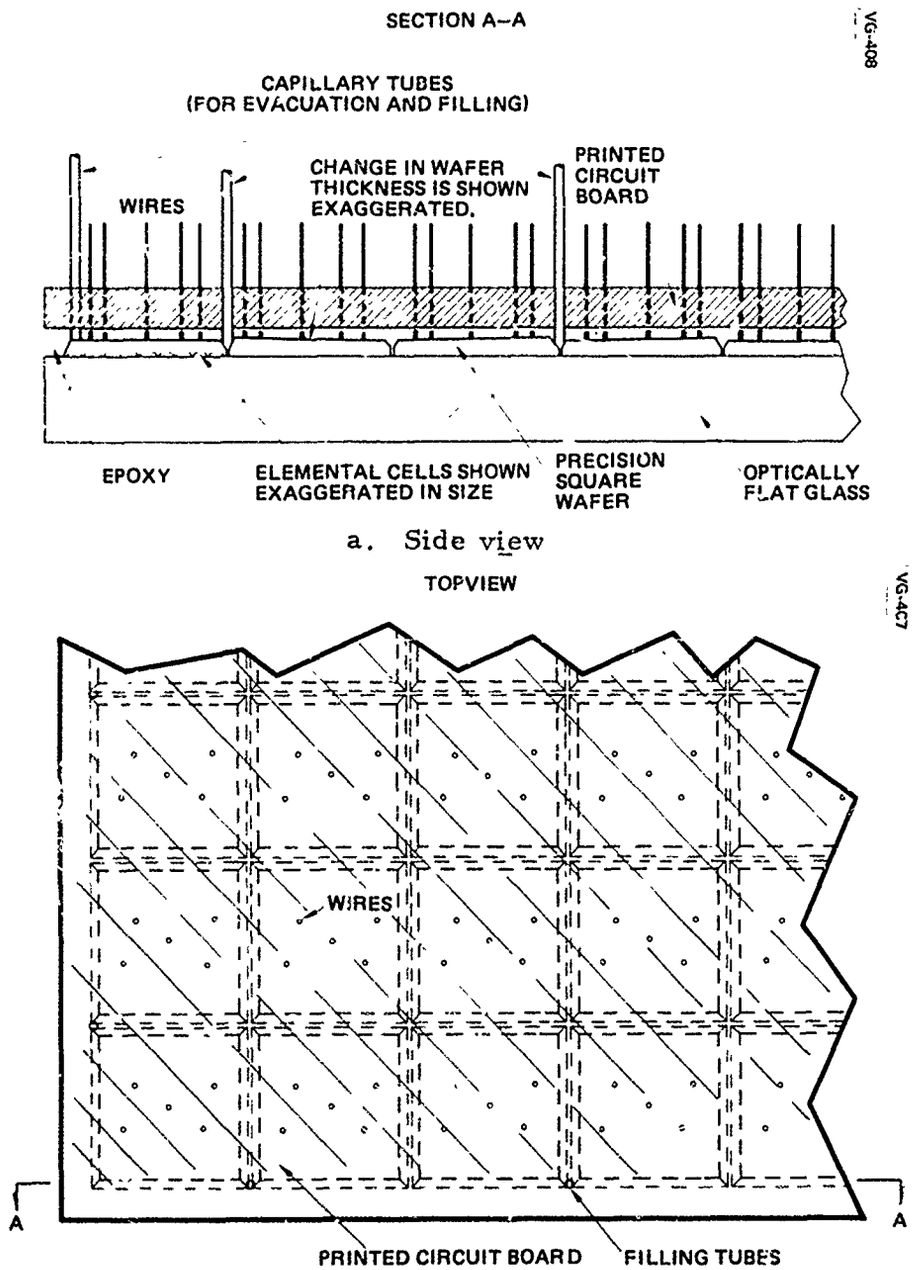


Figure 101. Assembly of self-contained modules.

of the display chip. Connections at the rear of the chip are facilitated by a conductive intraconnection pad positioned on the back side of the silicon chip so as to intersect each laser-drilled hole.

The resulting self-contained modules are assembled into a mosaic array in a manner identical to that described in the previous section and illustrated in Figure 101.

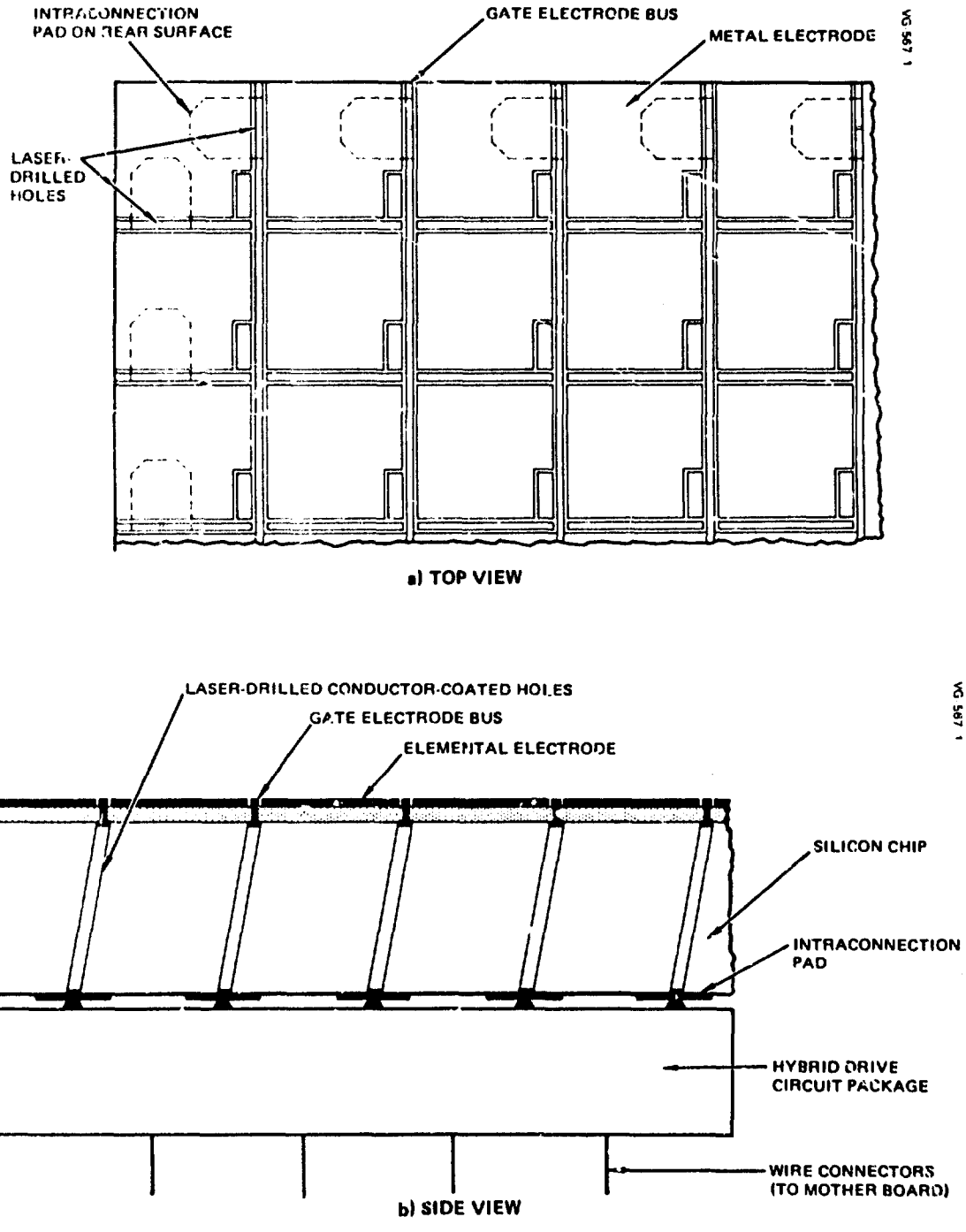


Figure 102. Conductor-coated hole technique for self-contained module.

Transistor Feed-Through

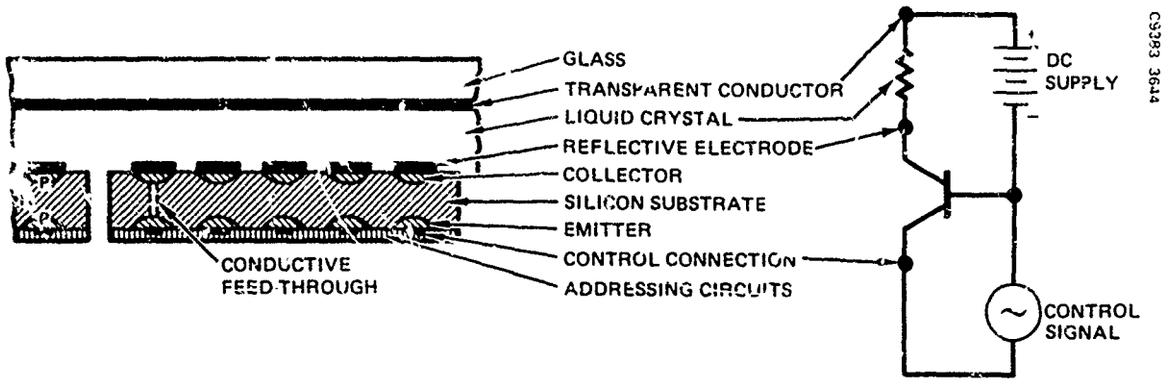
In the "feed-through" approach to self-contained modules, a conductive path is present in the silicon chip for each elemental electrode in the display matrix. The addressing circuits are fabricated on the rear surface of the wafer and the conduction paths through the silicon wafer connect to the reflective electrodes on the front surface.

The technique requires that diffusions be made on both the front and back surfaces of the wafer, as shown in Figure 103a. If a potential is applied to the rear surface diffusion area, or emitter, by the X-Y electrode busses, charges are injected into the silicon at that point. By providing suitable load resistance in the liquid crystal layer, these charges are attracted to the higher potential of the front surface diffusion, or collector, area. In effect, this transistor feed-through is equivalent to a common base amplifier circuit. The base of the transistor (center of the chip) is grounded, the input signal is fed into the emitter (rear of the chip), and the output signal is received at the collector (front of the chip).

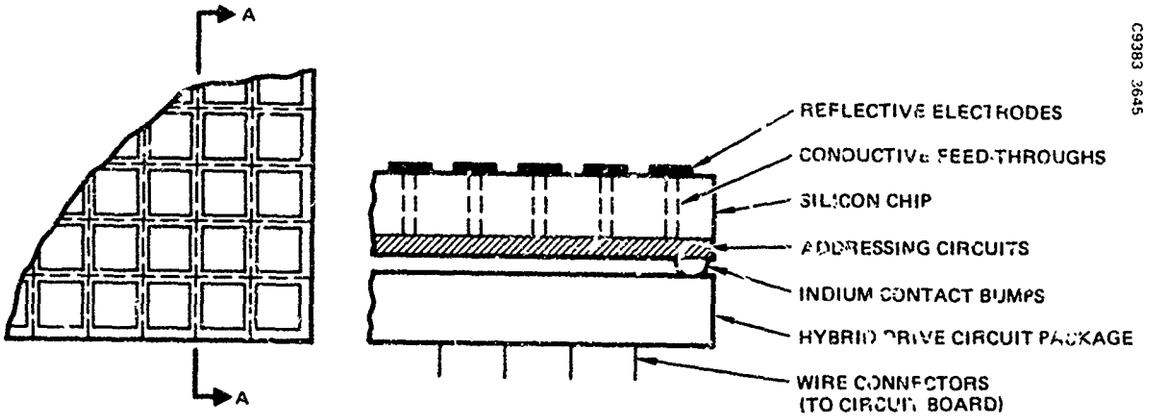
Figure 103b shows how the transistor feed-through substrate would be connected in the rear to the hybrid circuit drive package, to form the self-contained modules. The self-contained modules are assembled into a mosaic array in the same manner as described previously and illustrated in Figure 109.

Deep Etched Holes

This final technique is similar to the transistor feed-through in that a connection is made between every electrode on the front surface of the module, and its addressing circuit on the rear surface. In this case, holes are etched through the silicon substrate of the standard MOS-FET array just prior to oxide deposition (see Appendix B). The substrate would then be reversed, and these holes back filled with conductive material. Thus a direct connection would be established between the circuits on the front and rear surfaces of the substrate. All the holes on a module would be etched simultaneously, and a 100 x 100 element module would have 10,000 holes. A cross section of the contacts formed by this technique is shown schematically in Figure 104.



a) TRANSISTOR FEED-THROUGH CONCEPT AND EQUIVALENT ELECTRICAL CIRCUIT



b) PARTIAL TOP VIEW AND CROSS SECTION A-A AFTER ASSEMBLY

Figure 103. Transistor feed-through technique for self-contained modules.

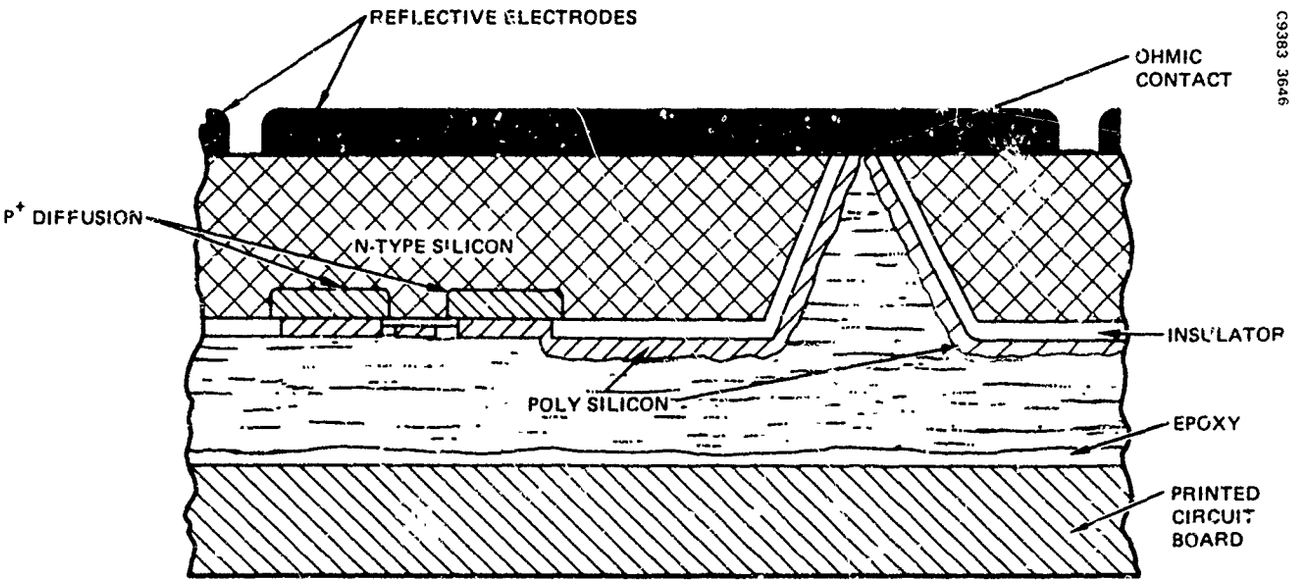


Figure 104. Deep etched hole technique.

TESTING AND TRADE-OFF

Six techniques for the assembly of individual modules into large array liquid crystal displays have been presented. These techniques are shown in Figure 105 and can be classed into three groups: those suitable for an interconnected approach — bridging, and wrap-around with side connections; those suitable for a self-contained approach — transistor feedthrough, and deep etched holes; and those suitable for either approach — conductor-coated holes, and wrap-around with rear connections.

In the preliminary trade-offs of these techniques, four factors were considered:

- Cost of experimental development
- Time required for experimental development
- Estimated production costs and complexity
- Ultimate flexibility of technique

Preliminary Trade-Offs

Long development times, and high development costs eliminated the transistor feed-through, and conductor-coated hole techniques from consideration. While the flexibility of the transistor feed-through approach is estimated to be high, it is beyond present state-of-the-art techniques. The major problems of this technique are: the requirement for diffusions on both sides of the

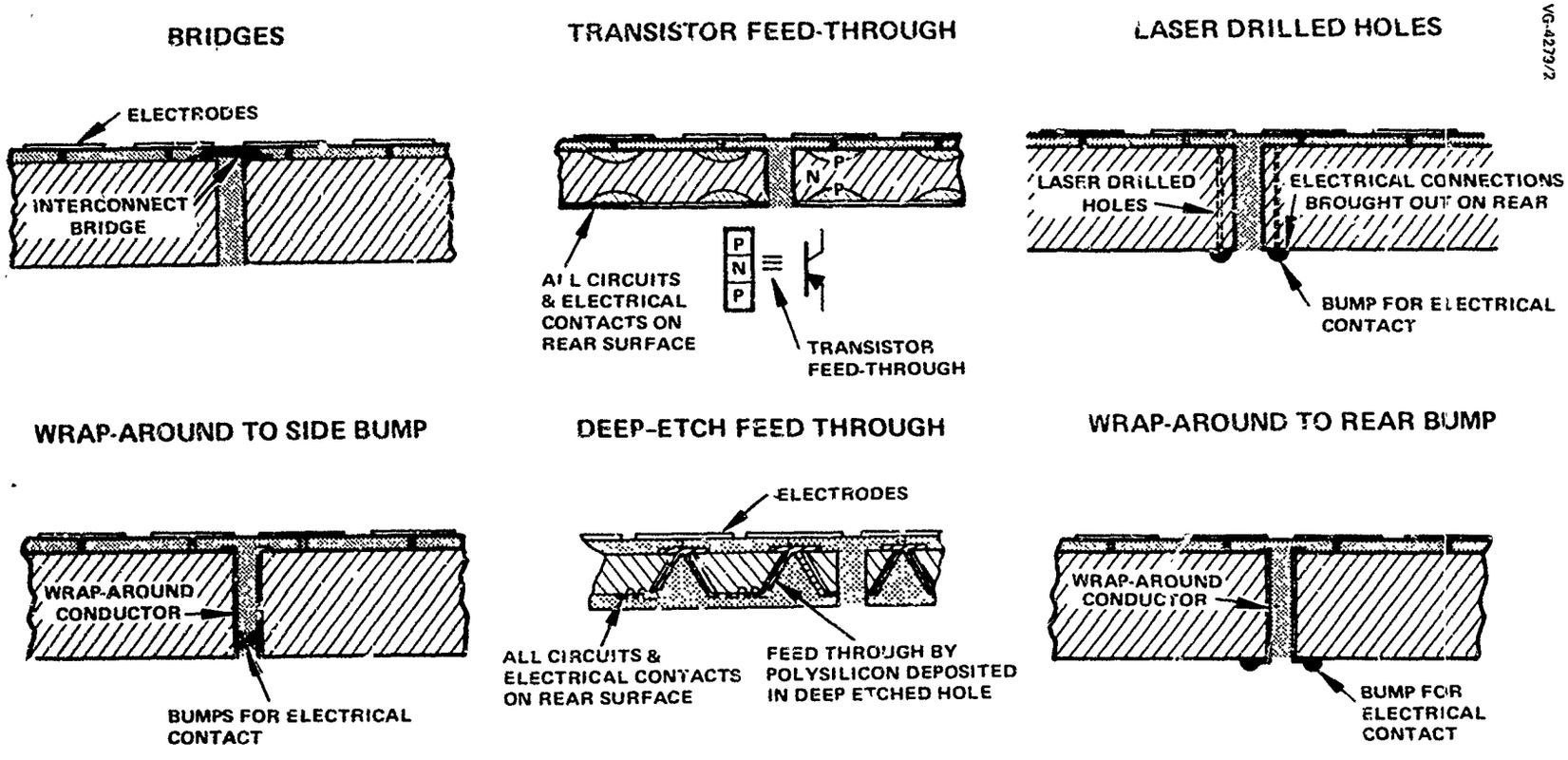


Figure 105. Alternate assembly techniques.

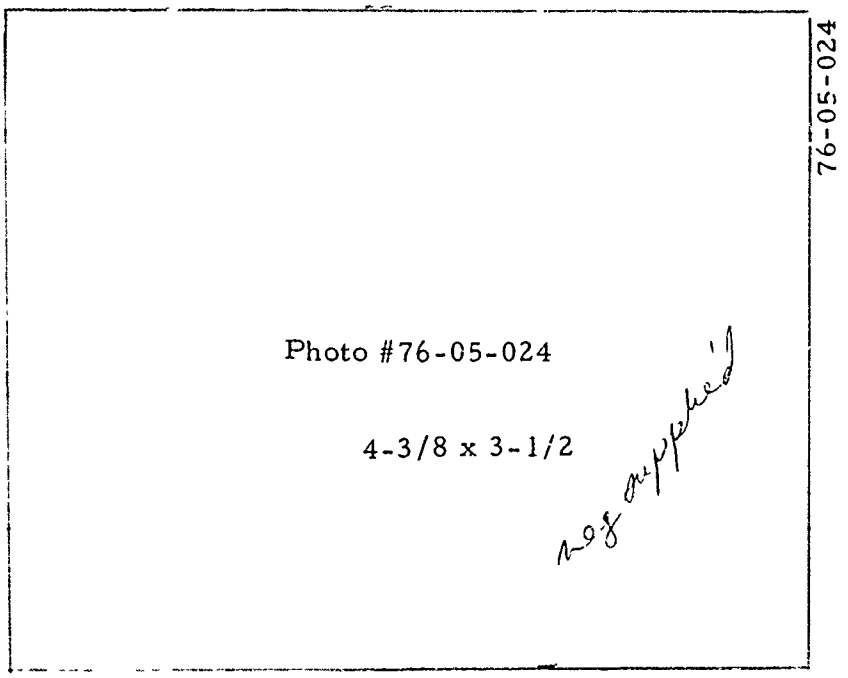
wafer; and impedance mismatch. Diffusion on both surfaces of a silicon wafer is not an impossible concept, but unattractive at present because of the extremely low yields predicted. The impedance mismatch results from the fact that optimum scattering efficiency in the liquid crystal requires a long pulse of relatively small current, and the feed-through technique would deliver a short pulse of high current. Thus, each picture element would require an additional transistor current amplifier for impedance matching.

The conductor coated hole approach uses existing laser drilling techniques for forming the holes. However, these techniques have only been successfully applied to semiconductor wafers that require few holes. For the liquid crystal display modules, each wafer would require 400 or more holes drilled in it, and the inspection and testing of these in itself is a major problem.

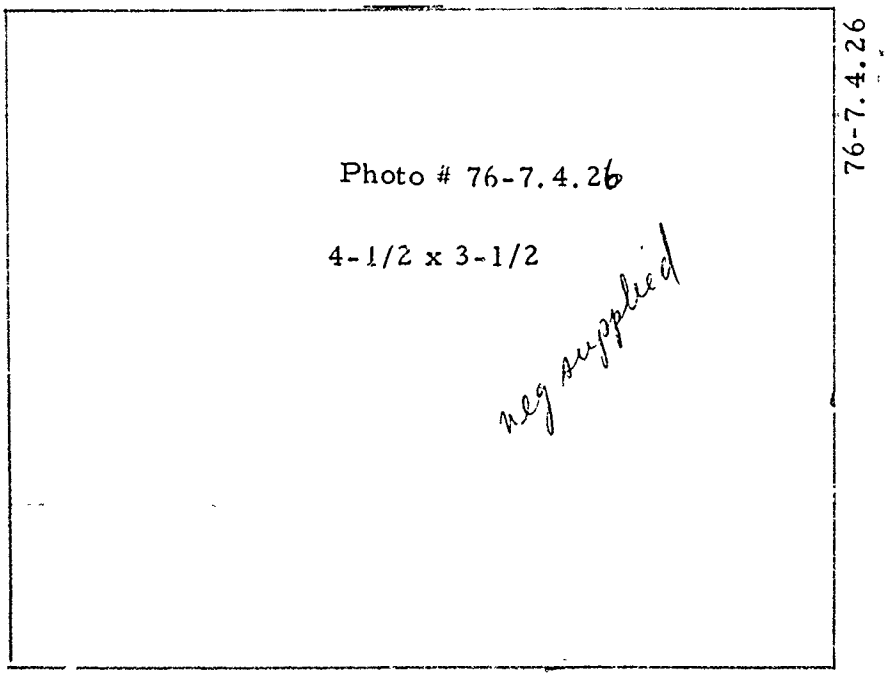
The deep-etched hole approach, like the transistor feed-through approach, requires processing both sides of the semiconductor wafer. The former approach, however, does not require the same level of complexity and control that the latter does. In addition, the practicality of the deep-etch technique could be developed independently, even though completion of the technique would require fully processed wafers. Various etchants and etching times have been experimented with, and the best results are present in Figure 106a and b. As inspection shows, the quality of the holes was not sufficient to warrant additional work, especially in view of the long development time expected.

Both wrap-around conductor approaches require about the same development time and costs. However, the increased flexibility of the rear bump technique, in addition to the fact that it does not require the same precision of side preparation as the side bump technique, leads to its choice for experimentation.

The bridging approach lacks the flexibility of the wrap-around rear bump approach, but also requires only moderate development costs and relatively short development times. For this reason, it too was chosen for experimentation. The approach choices, as well as a summary of the preliminary trade-offs, are presented in Table 12.



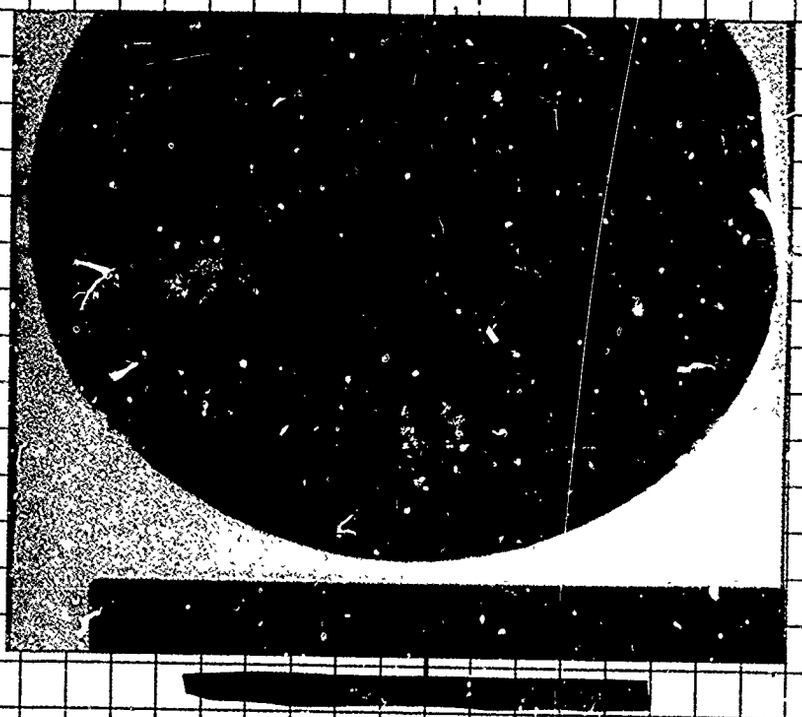
a. Top view microphotograph



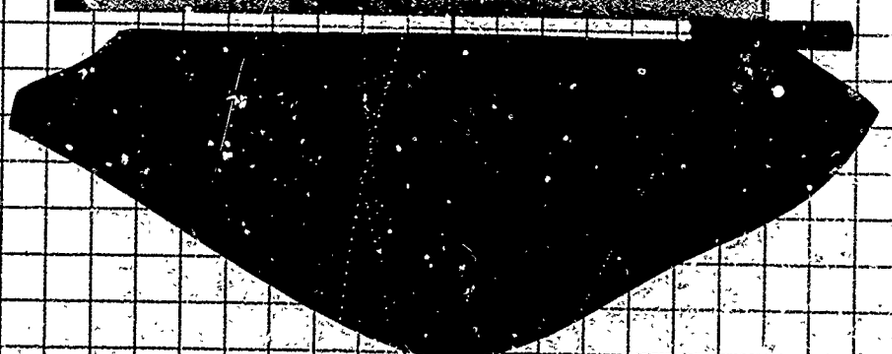
b. Scanning electron microscope picture

Figure 106. Results of experiments to produce deep etched holes.

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TABLE 12

PRELIMINARY APPRCACH TRADE-OFFS

	Interconnect Approaches		Self-Contained Approaches		Convertible Approaches	
	Bridging	Wrap-Around Side Bumps	Transistor Feed-Through	Deep-Etched Holes	Conductor Coated Holes	Wrap-Around Rear Dumps
Experimental Development Costs	Moderate	Moderate	High	High	High	Moderate
Experimental Development Time	Short	Short	Long	Long	Long	Short
Estimated Production Costs	Moderate to High	Modera'e	Moderate to High	Moderate	Moderate	Low to Moderate
Predicted Flexibility	Low	Low	High	Moderate	Moderate	High
Chosen for Experimentation?	Yes	No (see rear bump)	No	Some	No	Yes

Part Task Testing

To provide additional data on the relative advantages and disadvantages of the bridging and wrap-around techniques, experimental testing was undertaken to determine the feasibility of complete fabrication using these techniques.

Bridging

The key item required for the success of the bridging approach was a technique for filling up the voids between modules such that the metal deposited during the bridge deposition would be mechanically supported. A gravity flow process was tried first. The wafers were positioned face down on a flat surface, with filling material placed on the back sides and allowed to flow down between them. Adherence to the mounting plate was to have been prevented by coating it with a substance that could be easily dissolved after the array had been assembled. However, the experiments were not successful as the removal of the silicon modules could not be accomplished reliably. In fact, one complete mounting had to be scrapped because the modules could not be removed from their surfaces.

The technique that was found to be successful used capillary action to fill the voids between modules. Prior to assembly, small grooves were cut in the mounting plate in locations that would lie directly under the module junctions when the array was assembled. The modules were then mounted

on the plate using a double sided sheet epoxy, such as able stick, after having been carefully aligned to one another. At the completion of this step, the grooves underneath the module junctions were filled with an epoxy of the right viscosity. This epoxy flowed by capillary action down the grooves and up into the voids between the modules. The surface tension on the epoxy fluid formed a slight hump in the junction, but this leveled out as the epoxy shrunk upon curing.

Thus, it was shown that the biggest unknown associated with the bridging technique could be overcome. Further work is required to optimize the epoxy materials in terms of their mechanical properties, and their chemical compatibility with liquid crystal materials. Contamination is also a concern, however, the inclusion of a smoothing layer envisioned for future displays would place a protective barrier between the epoxy fill and the liquid crystal.

Wrap-Around

The key item for success with the wrap-around approach was finding a technique for forming the conductors around the edges of a module. The basic concept was simple enough, but it had never actually been done. The process involves depositing an insulator along the module's edge, and then depositing a metallic conductor on the top and side surfaces using a physical mask. (Photoresist masking was considered impossible because of the problems involved with depositing a coating of uniform thickness and exposing it.) Several insulator materials and application techniques were tried before a working combination was found. For example, dipping the module into a polyimide solution and curing the adhering film, and placing the modules in an anodizing bath to form a thick oxide coating were tried before an approach employing a vacuum deposited SiO_2 coating was settled on.

Having formed a suitable insulator, the next step was to deposit metallic conductors around the edge. The concept here was to use a U-shaped metal mask (per Figure 107) and to rotate the module along the edge axis during the deposition cycle. Initial attempts were successful, though difficulty was encountered in coating around the sharp corner at the front surface edge. However, by lightly polishing the edge of the module on a buffing wheel, the corner was rounded slightly and good electrical conductivity was assured. The net result of these efforts is presented in Figure 108, which shows that the wrap-around approach could be completed successfully.

4 3/4 x 3 3/4

Figure 107. Metal mask prior to bending.

VG-4280/1

2 1/16 x 1 9/16

Figure 108. Experimental trial.

Final Tradeoff

The processing steps required to implement the bridging technique and the wrap-around conductor with bottom contact technique are compared in Table 13. It is evident that they are about equal in complexity, and that neither requires a major advance in state-of-the-art. The bridging technique is slightly more straightforward in that it uses vacuum deposition techniques which have been well developed for the production of shadow mask and storage tubes. However, the experiments with wrap-around conductors indicate that they are not as difficult to fabricate as first thought. Either the bridging technique or the wrap-around conductor technique with bottom contacts is adaptable to building an interconnected display. The wrap-around conductor with bottom bump technique,

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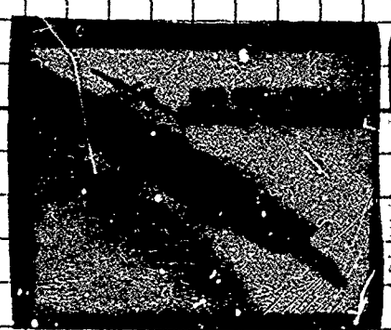


TABLE 13

COMPARISON OF REQUIRED PROCESSING STEPS

Wrap-Around Technique	Commonality	Bridging Technique
• Deposit insulator using metal mask		• Mount modules to mounting surface
• Deposit wrap-around conductor using metal mask		• Fill voids between modules
• Deposit indium bumps on circuit plate		• Insulate edges
• Mount modules to circuit plate		• Deposit metallic bridges using metal or photoresist masks
• Deposit insulation/smoothing layer		• Deposit insulation/smoothing layer
• Cut holes in insulation/smoothing layer		• Cut holes in insulation/smoothing layer
• Deposit and define reflective electrode structure		• Deposit and define reflective electrode structure

however, does offer several potential advantages that are not matched by the bridging approach:

1) It reduces the impact of interconnect failures on display yield. The critical deposition step is accomplished earlier in the display fabrication sequence; hence, a failure at that point ruins only a single module rather than a whole array of modules.

2) It does not rely on capillary action to fill the gaps between modules, as does the bridging approach. Therefore, it eliminates the difficulties and uncertainties associated with extending the capillary filling procedure to large display sizes.

3) It eliminates the electrode bus resistivity as a limiting factor on display size. As the length of the signal busses is increased, signal attenuation becomes more severe. With the wrap-around approach to interconnecting modules, redundant electrode busses can be placed on the mounting plate to insure sufficiently low resistance busses.

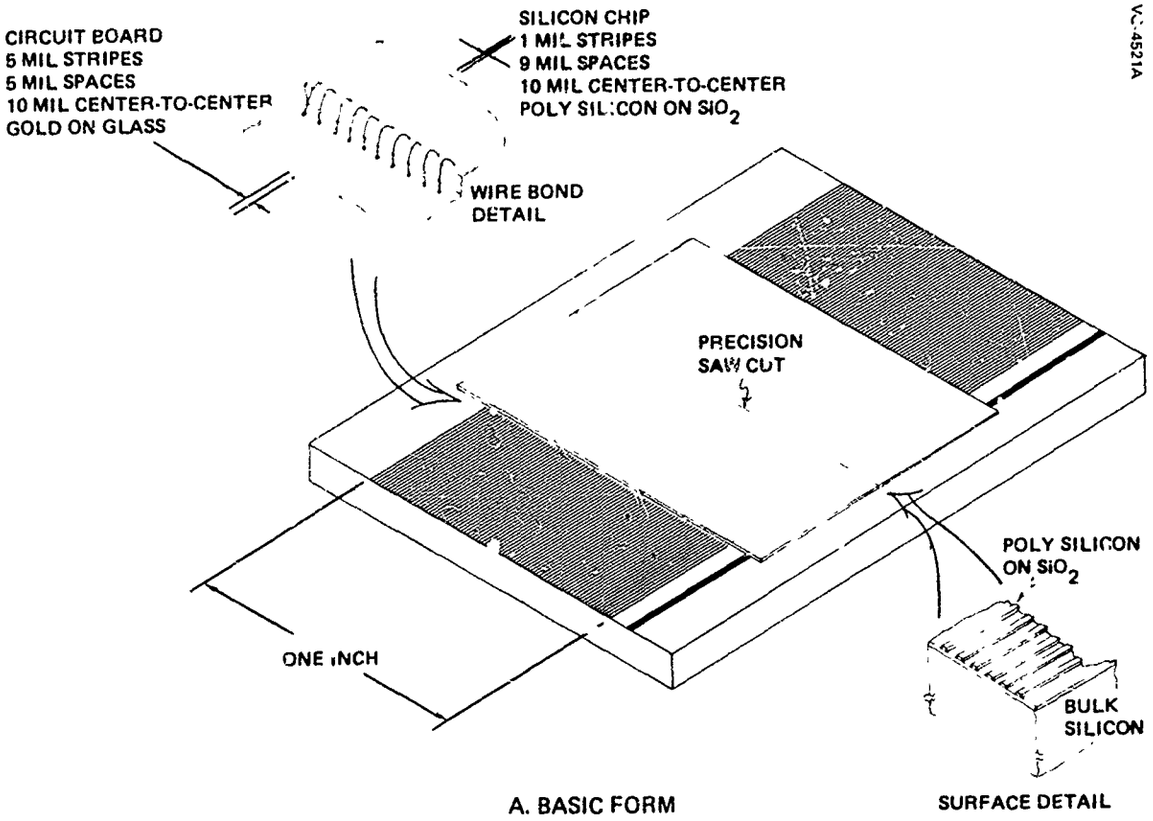
In summary, the previous technical discussions pointed out two basic approaches for building up a mosaic array of display modules. The interconnect approach places the drive circuitry around the periphery of the display, and the signals to be sent to the modules in the center of the array are carried in from the edge by the electrode busses of the peripheral modules. With the self-contained module concept, the drive circuitry for each module is placed behind that module and the drive signals are brought from the rear to the front of each individual module by some front-to-back connection scheme. The interconnect approaches all have the advantage that they can be implemented with a minimum of new development work and new tooling. The self-contained module approaches, however, promise to make possible the building of different size displays by merely assembling a different number of modules. For example, if a standard module had a 3:4 aspect ratio, a 3:4 aspect ratio display could be built by assembling a 3 by 3 array of modules, and a square display could be built by assembling these same size modules into a 4 by 3 module array. The same basic module could be used to build displays for both the commercial and military

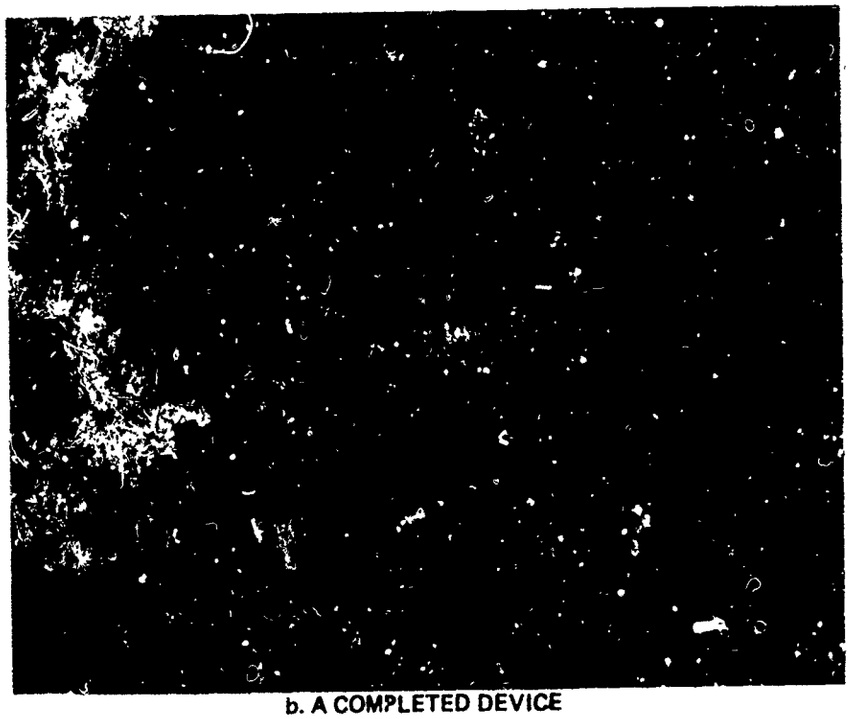
markets, and so would establish a broad and sizable market for the liquid crystal television display by reducing manufacturing costs to levels where it can compete with the existing cathode ray tube technology. The cost of producing a liquid crystal display in the future is going to be primarily dependent upon the cost of producing the semiconductor wafers for driving the liquid crystal material itself. Thus, it was concluded that the wrap-around technique would be implemented as a conceptual model for mosaic array displays.

CONCEPTUAL MODEL FABRICATION AND TESTING

A conceptual model is a device fabricated at minimum expense to show how modules could be interconnected for an actual display application. It is not an operating display, but merely a vehicle for testing a proposed interconnect technique. The basic conceptual model is illustrated schematically in Figure 109a, and a photograph of a completed unit is shown in Figure 109b. Two large (1-inch square) silicon chips were mounted adjacent to one another so as to simulate two adjacent display modules. The silicon chips were precision sawed prior to mounting so their edges could be positioned exactly, in a manner analogous to that planned for the actual modules. The structure on the surface of the silicon chips includes the lines to be interconnected as well as other elements which are irrelevant to this task. (The existing metalization layer mask was used to form the polysilicon lines, however, it would have to be modified to work for an actual interconnected display.) The conceptual model devices fabricated in this manner made it possible to study and demonstrate interconnect techniques suitable for making module-to-module connections using the present display density of 100 conductors per linear inch.

In fabricating the conceptual module devices, a procedure for forming the contacts between the wrap-around conductors on the module and the underlying printed circuit board had to be established. Aligning the wrap-around conductors to the lines on the silicon modules was easily accomplished by visually aligning the metal mask used for the conductor deposition. It was necessary to build three devices before success was achieved, and each of those trials will now be discussed in detail.





b. A COMPLETED DEVICE

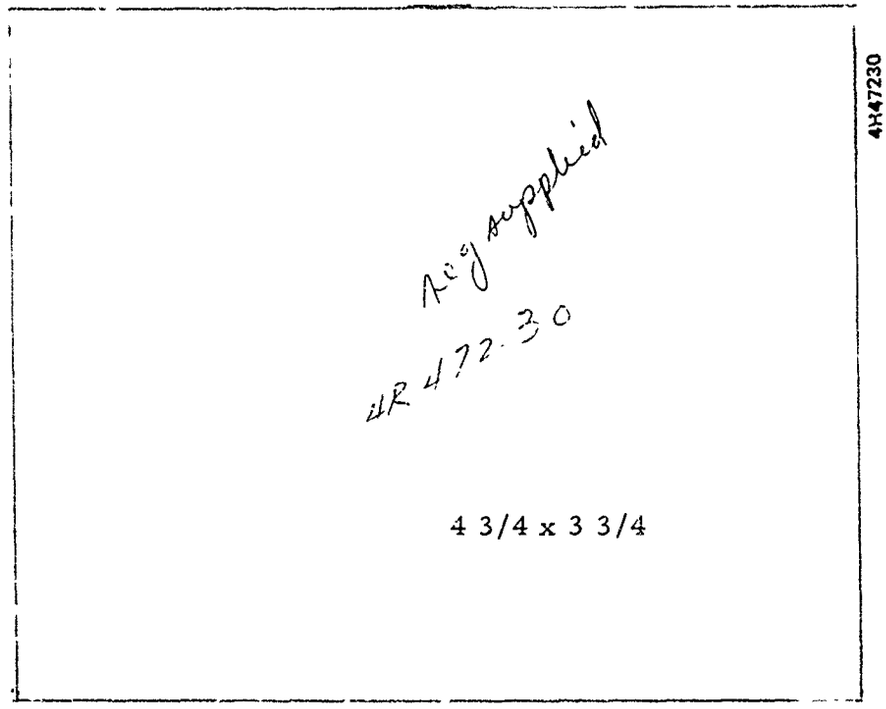
Figure 109. Interconnect conceptual model.


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MIL STRIPES
MIL SPACES
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GOLD ON GLASS
WIRE BOND DETAIL
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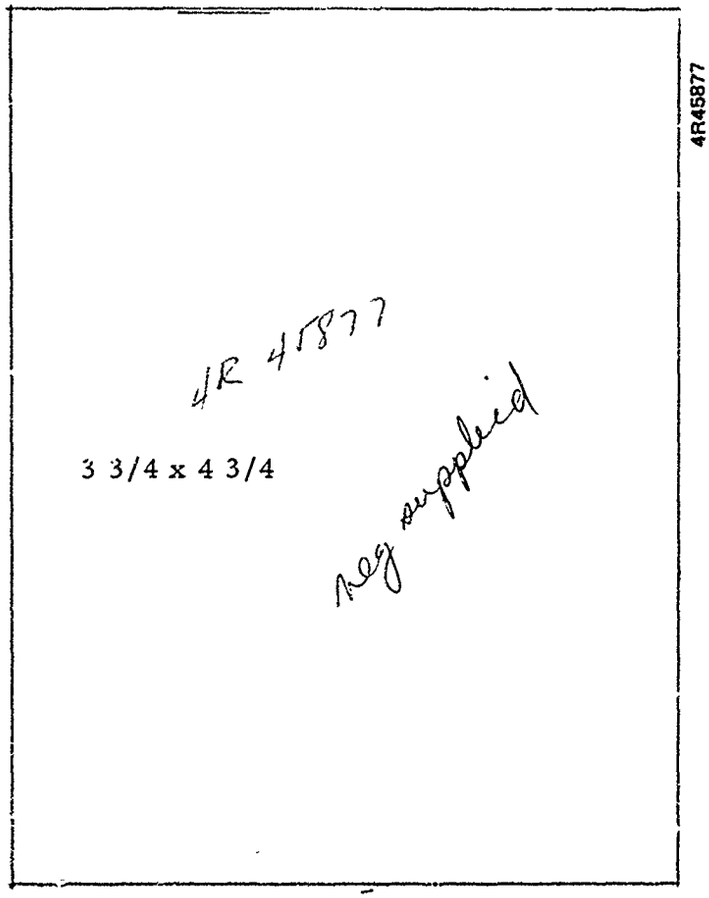
A conductive elastomer was used in the first conceptual device to provide the electrical contact between the wrap-around conductors and the underlying printed circuit substrate. Conductive elastomers are being developed to speed the assembly of electronic watches and calculators, and when compressed they have the characteristics of high lateral resistivity and low transverse resistivity. The photographs of device No. 1 in Figure 110 show how the elastomer was positioned under the modules. To insure compression of the elastomer, the modules were to be epoxied into place while under pressure. Unfortunately, the modules were not rigid enough to provide the required contact pressure or prevent distortion of the module's surface. As a result, electrical conductivity was established in only a few places.

The second conceptual device attempted to form the required electrical contacts by using indium deposited on top of the wrap-around conductors. In this manner, the feasibility of the wrap-around side bump technique could be explored at no additional cost. Unfortunately, the metal mask had been made from an easily worked material which had deteriorated to the point where the small bars between the spaces were no longer thick enough to prevent the indium from falling between adjacent conductors and shorting them. (It had been expected that the mask would be adequate for the limited number of tests to be conducted; however, more tests were required than anticipated, and it deteriorated to a point no longer satisfactory.) The shorting, where the indium flared out under the mask, can be seen in the microphotograph of device No. 2 presented in Figure 111. However, even though this device failed to work, it provided us with enough experience in the deposition of indium to convince us that we were on the right track.

A third conceptual device was assembled after the new metal mask had been obtained and it is shown in Figure 112. This device also used indium, but the indium was deposited on the printed circuit mounting plate instead of the module. To assure good contact, the indium was deposited on top of a layer of chromium. Indium forms balls when deposited on chromium, like water on an oil soaked surface, and these balls ensure contact across the micron-thick gaps that remain when the two surfaces are mated. Microphotographs of this third device appear in Figures 113 and 114.



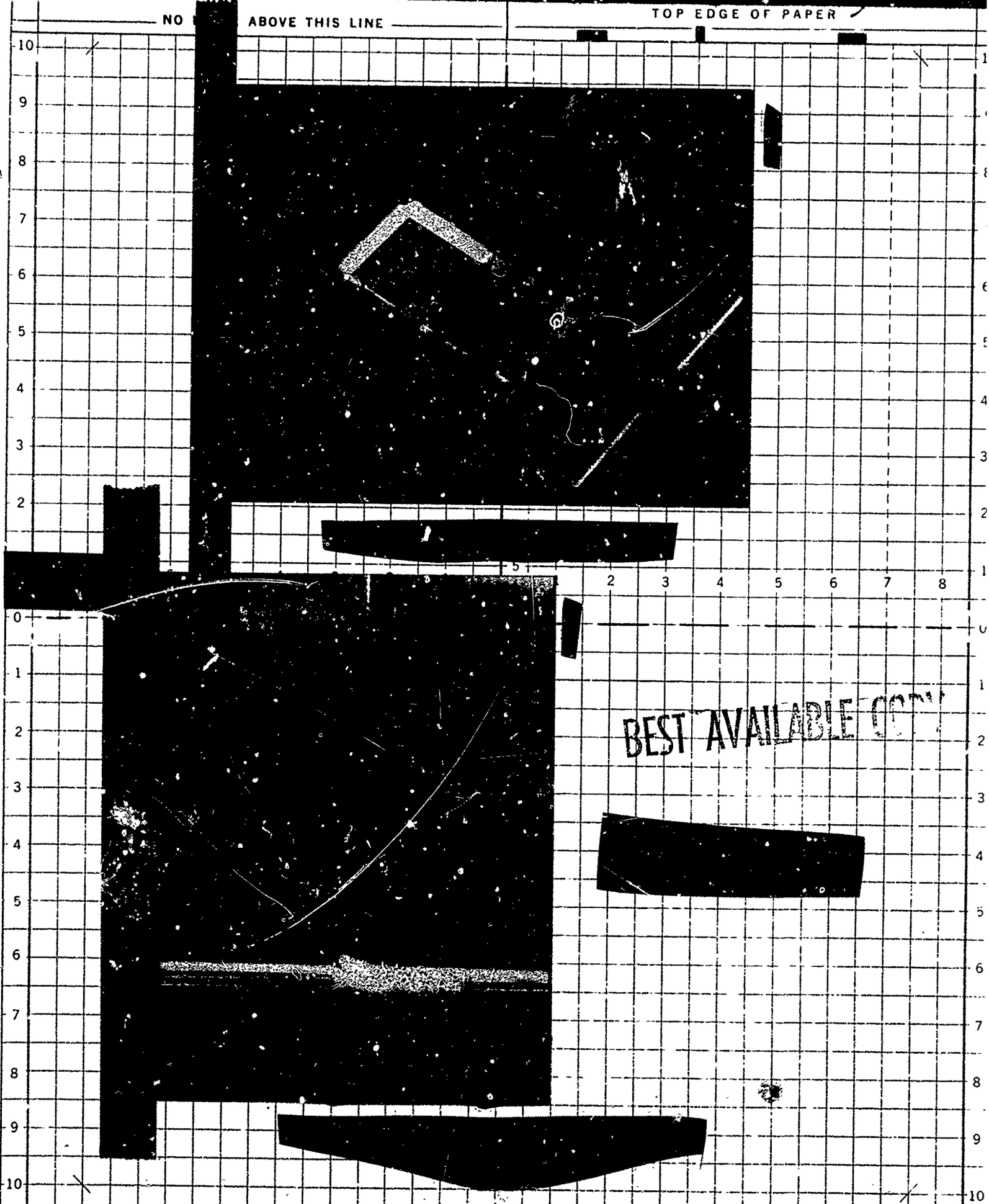
a. Module position on printed circuit mounting surface.



b. Conductive elastomer positioned under junction.

Figure 110. Conceptual model device No. 1.

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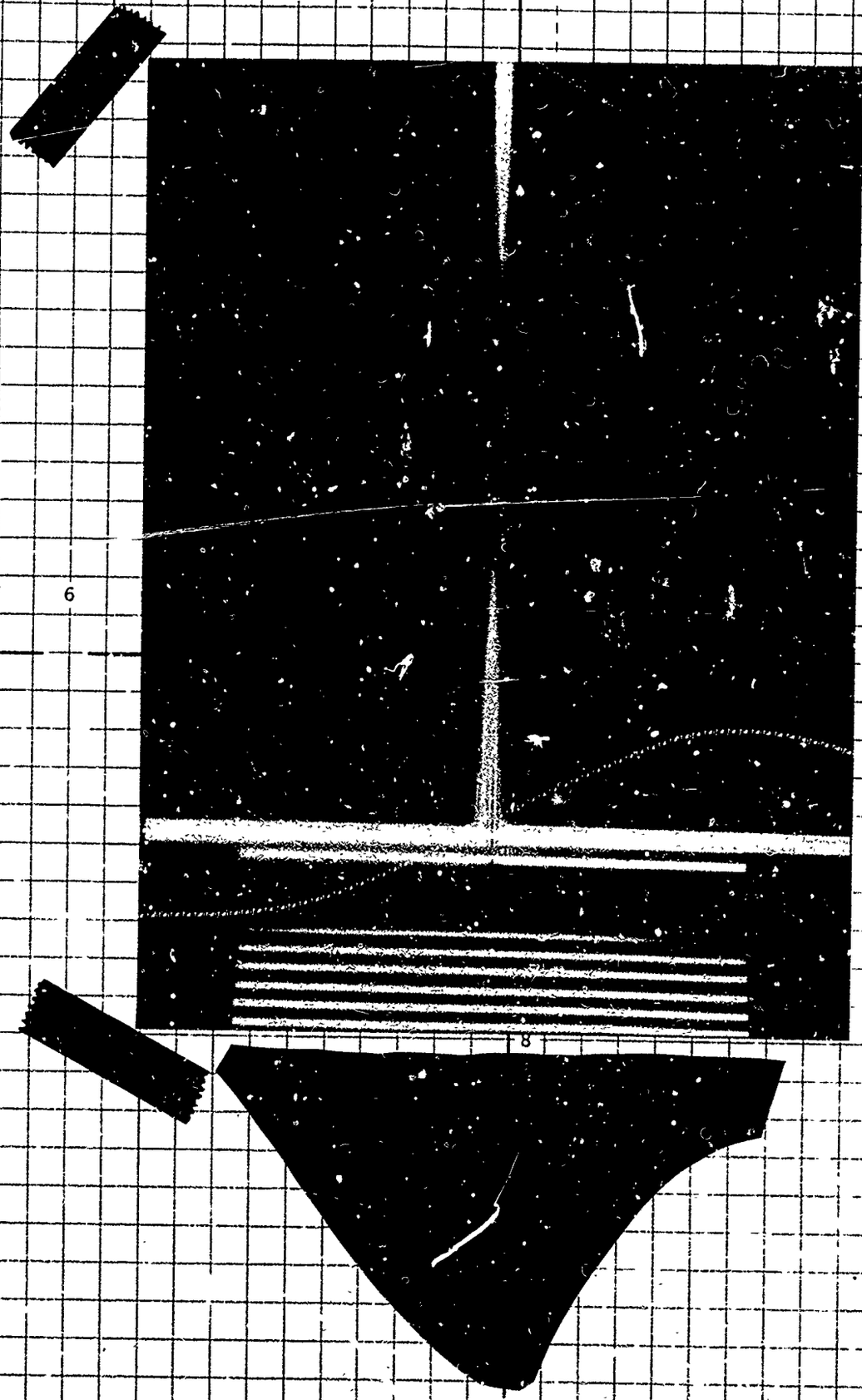
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Figure 111. Microphotograph of conceptual model device No. 2.

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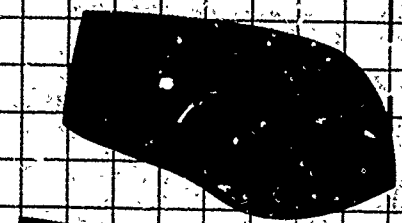
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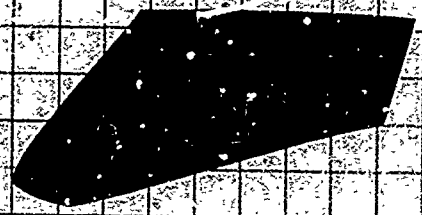
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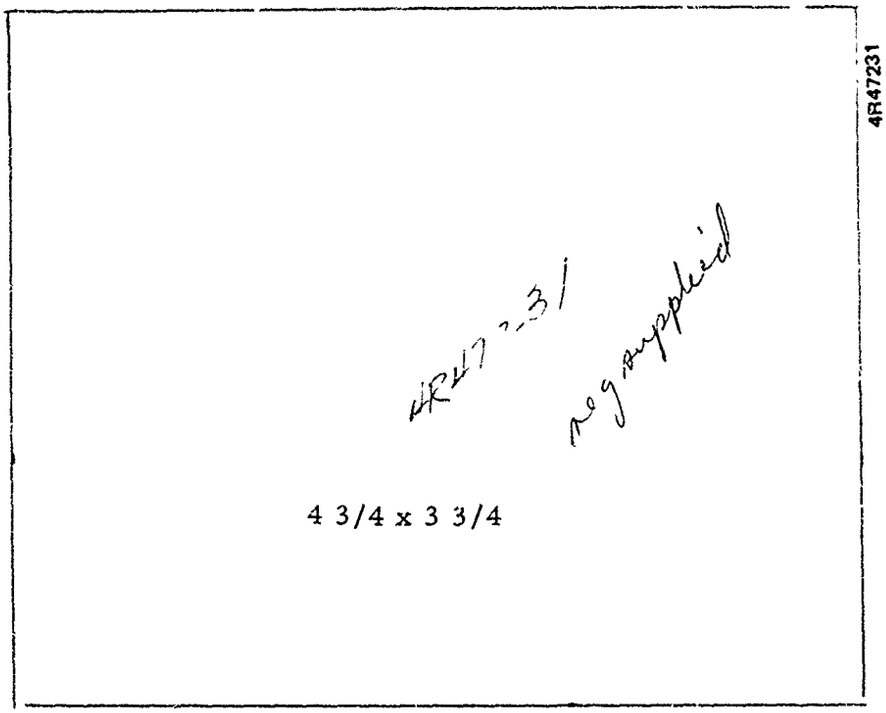


Figure 112. Conceptual model device No. 3.

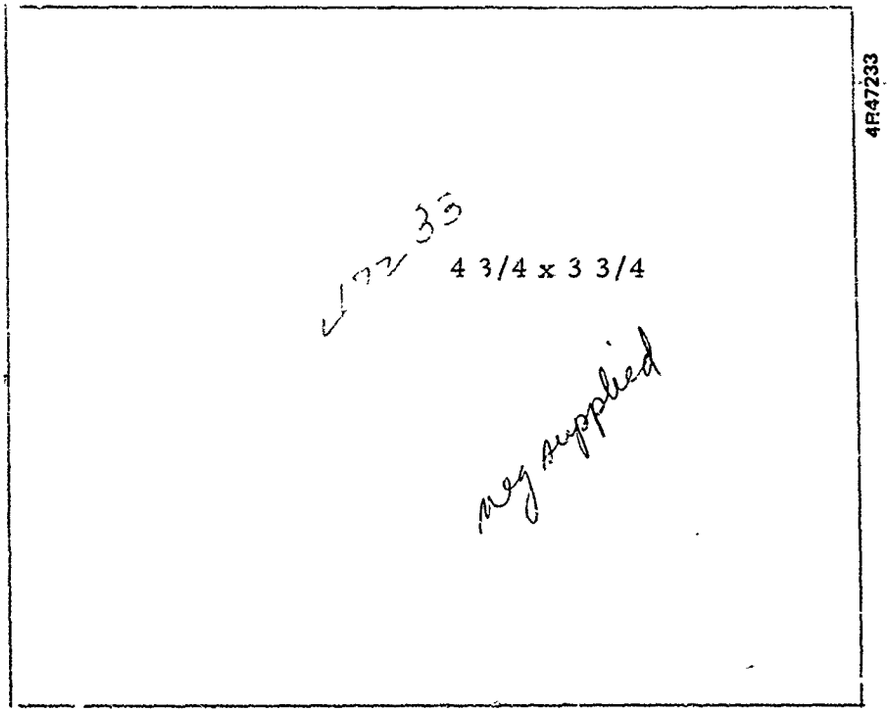
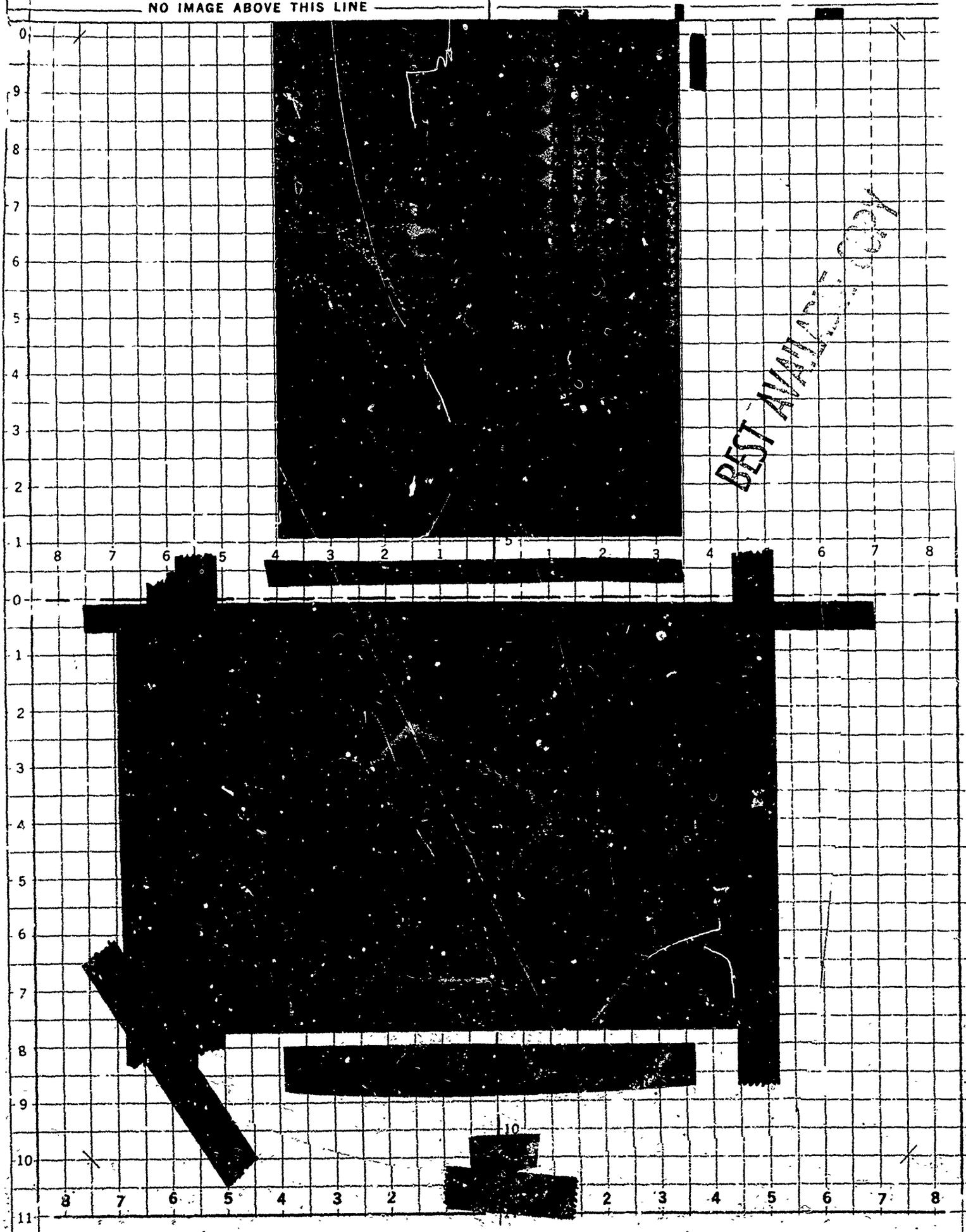


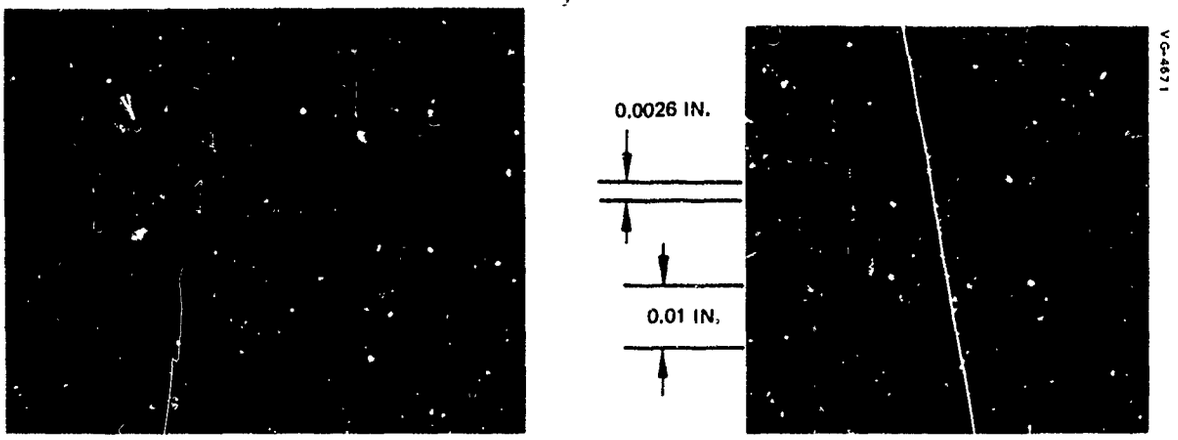
Figure 113. Conceptual model device No. 3 showing detail of backlighted junction.

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Top View Bottom View

Figure 114. Microphotographs of conceptual model device No. 3.

This third device was tested for continuity shorts, and opens and shorts to substrate using a Temptronic Corp. TP-36 single probe capacitance versus voltage test station, a Tektronix 577 curve tracer, and a conventional ohmmeter. The data is presented in Table 14. A resistance of approximately 1.5×10^5 ohms between two ends of the same line indicates a good conductive path. A resistance of greater than 15×10^5 between two adjacent lines indicates satisfactory line isolation. Examination of the data shows that thirteen of the 100 lines are perfect.

The nature of the shorts to adjacent lines was investigated in detail, and it was found that they are due to spreading of the aluminum wrap-around conductors at the edge of the chip. The amount of spreading is related to the juxtaposition of the silicon-chip and the metal mask and to the separation width between the holes in the metal mask. The masks were initially designed to have the separation distance equal to the hole width, but as a result of the overcutting associated with the mask fabrication process, the separations between the holes in the metal mask were reduced to three thousandths of an inch in width. It is now clear that if these dimensions are modified, the likelihood of adjacent line shorts would decrease to near zero, without any other changes in the processing or fabrication procedures.

The large number of opens occurring in lines 50 through 100 were also investigated in detail. Microscopic examination of the model showed that these opens were due to a spreading of the epoxy (used to hold down the silicon chips) over the printed circuit lines on the mounting plate. This epoxy insulated

NO IMAGE ABOVE THIS LINE

TOP EDGE OF PAPER

BEST AVAILABLE

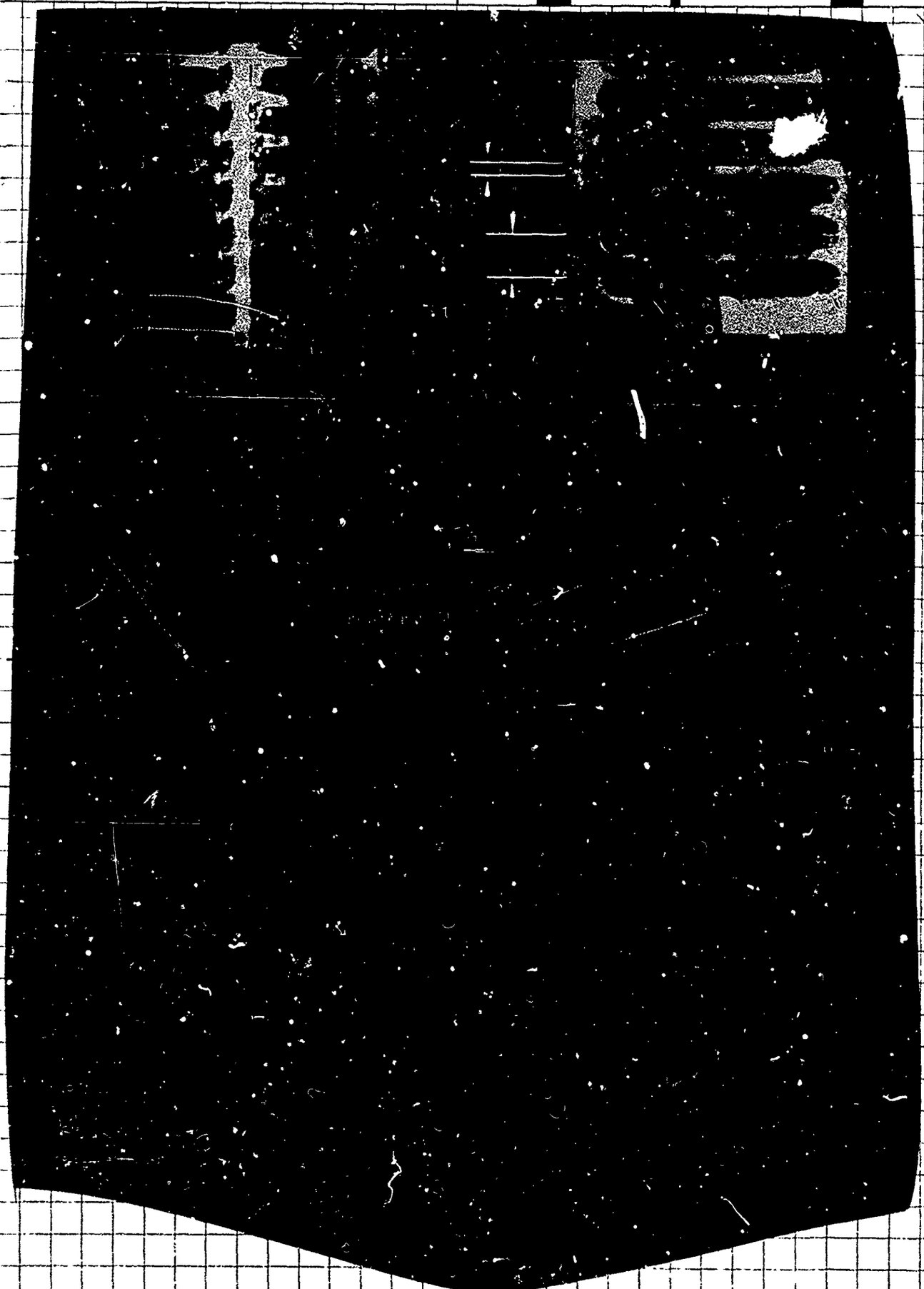


TABLE 14

INTERCONNECT CONCEPTUAL MODEL DEVICE NO. 3 TEST DATA

(Measured Resistance = Indicate Value x 10^5 Ohms)

Lines	Ohms	Lines	Ohms	Lines	Ohms	Lines	Ohms	Lines	Ohms	Lines	Ohms	Lines	Ohms	Lines	Ohms
1 to 1	1.5	13 to 14	20	26 to 26	1.5	38 to 39	1.5	51 to 51	1.5	63 to 64	50	76 to 76	30	88 to 89	32
1 to 2	19	14 to 14	1.7	26 to 27	31	39 to 39	1.5	51 to 52	1.4	64 to 64	23	76 to 77	41	89 to 89	45
2 to 2	14	14 to 15	1.8	27 to 27	1.45	37 to 40	1.5	52 to 52	13	64 to 65	13.5	77 to 77	40	89 to 90	50
2 to 3	28	15 to 15	1.4	27 to 28	40	40 to 40	1.6	52 to 53	12	65 to 65	22	77 to 78	50	90 to 90	15.5
3 to 3	28	15 to 16	12	28 to 28	1.55	40 to 41	1.65	53 to 53	10.8	65 to 66	30	78 to 78	50	90 to 91	15.5
3 to 4	40	16 to 16	200+	28 to 29	30	41 to 41	1.5	53 to 54	10.5	66 to 66	19.5	28 to 29	21	91 to 91	8
4 to 4	38	16 to 17	200+	29 to 29	1.4	41 to 42	1.6	54 to 54	10.5	66 to 67	30	79 to 79	200+	91 to 92	8.1
4 to 5	20	17 to 17	2.3	29 to 30	28	42 to 42	1.55	54 to 55	9.5	67 to 67	200+	79 to 80	200+	92 to 92	20
5 to 5	20	17 to 18	1.8	30 to 30	1.6	42 to 43	200+	55 to 55	5.6	67 to 68	200+	80 to 80	32	92 to 93	20
5 to 6	45	18 to 18	1.35	30 to 31	17	43 to 43	200+	55 to 56	6.5	68 to 68	50	80 to 81	200+	93 to 93	11
6 to 6	43	18 to 19	50	31 to 31	40	43 to 44	8.5	56 to 56	2.4	68 to 69	50	81 to 81	200+	93 to 94	10.6
6 to 7	1.45	19 to 19	1.5	31 to 32	200+	44 to 44	10	56 to 57	2.45	69 to 69	50	81 to 82	40	94 to 94	9.5
7 to 7	1.35	19 to 20	70	32 to 32	1.6	44 to 45	10	57 to 57	6.3	69 to 70	50	82 to 82	40	94 to 95	9.5
8 to 8	16	20 to 20	70	32 to 33	40	45 to 45	1.65	57 to 58	6.9	70 to 70	80	82 to 83	50	95 to 95	10.5
8 to 9	20	20 to 21	28	33 to 33	1.6	45 to 46	1.85	58 to 58	4.45	70 to 71	85	83 to 83	60	95 to 96	10.5
9 to 9	19.5	21 to 21	1.5	33 to 34	38	46 to 46	1.75	58 to 59	5	71 to 71	70	83 to 84	40	96 to 97	12.6
9 to 10	10.5	21 to 22	17	34 to 34	1.4	46 to 47	1.8	59 to 59	6.4	71 to 72	70	84 to 84	30	96 to 97	13
10 to 10	1.4	22 to 22	1.4	34 to 35	27	47 to 47	1.79	59 to 60	6.4	72 to 72	55	84 to 85	20	97 to 97	1.55
10 to 11	50	22 to 23	28	35 to 35	1.4	47 to 48	1.65	60 to 60	45	72 to 73	55	85 to 85	35	97 to 98	1.6
11 to 11	50	23 to 23	43	35 to 36	2.5	48 to 48	6.4	60 to 61	45	73 to 73	55	85 to 86	36	98 to 98	50
11 to 12	35	23 to 24	20	36 to 36	1.4	48 to 49	6.4	61 to 61	7.3	73 to 74	33	86 to 86	11	98 to 99	50
12 to 12	33	24 to 24	25	36 to 37	1.5	49 to 49	1.45	61 to 62	7.3	74 to 74	24	86 to 87	11	99 to 99	200+
12 to 13	1.4	24 to 25	19	37 to 37	7	49 to 50	1.55	62 to 62	1.4	74 to 75	45	87 to 87	18	99 to 100	200+
13 to 13	1.45	25 to 25	20	37 to 38	7.2	50 to 50	1.55	62 to 63	1.5	75 to 75	55	87 to 88	18	100 to 100	200+
		25 to 26	200+	38 to 38	1.4	50 to 51	1.5	63 to 63	9	75 to 76	36	88 to 88	38		

these lines from the wrap-around conductors and prevented electrical interconnection between the chips. In the future, this spreading will be avoided by using an ABLESTICK type material to better control epoxy thickness. When the number of defective interconnections is adjusted to take into account this epoxy problem, the success rate is increased to over twenty-five percent.

In summary, these conceptual models demonstrate a viable technology for achieving electrical interconnection between display modules.

CONCLUSIONS AND RECOMMENDATIONS

Several alternative techniques were investigated for assembling an array of semiconductor modules so as to make possible the fabrication of a large area liquid crystal airborne display. A bridging approach, and a wrap-around rear-connection approach were identified as having short term promise, and the key unknown steps in the fabrication of each were explored as partial task tests. The wrap-around conductor approach was selected for implementation in a conceptual model device, and its feasibility was shown. The project successfully established a technology base upon which further development of a large interconnected liquid crystal display can build.

A key achievement was the demonstration of conductive paths between the front and rear surfaces of silicon chips, using the wrap-around technique. This milestone makes it realistic to consider a totally modular approach to the fabrication of liquid crystal television displays. Displays of arbitrarily large size and resolution could be assembled by using an array of such modules.

The next step in the development of a large modular liquid crystal television display for airborne or ground applications is the assembly of an operational one-by-two module interconnected display like that shown in Figure 115. A display of this type would provide a vehicle for exploring the techniques for (1) accommodating the wrap-around conductors without interfering with the operation of the picture elements on the edge of the module; (2) insulating the wrap-around conductors from the overlying liquid crystal material, and (3) establishing data from which accurate yields, costs, and schedules could be predicted. The successful completion of a one-by-two module interconnected display would lead to the assembly of a

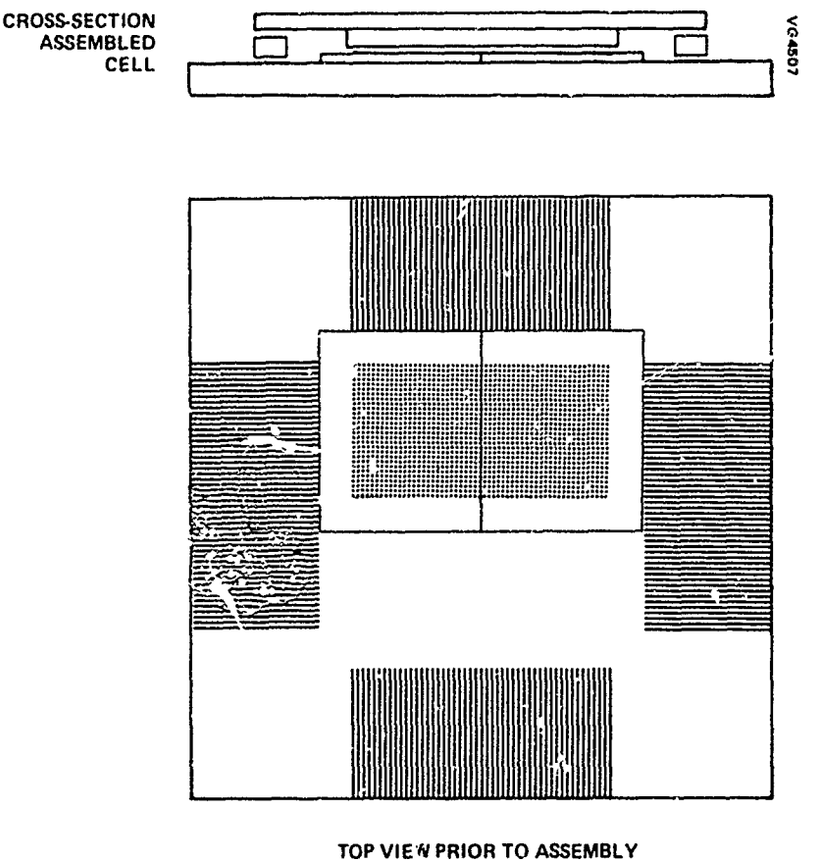


Figure 115. Operational 1 x 2 module interconnected display.

three-by-three module display which could be as large as 5-1/4-inches square if modules were cut from three inch diameter wafers. A 5-1/4-inch square display would present a larger display area than many of the present aircraft CRT displays.

SECTION VIII
CONCLUSIONS AND RECOMMENDATIONS

In conclusion, the feasibility of the liquid crystal airborne display technology has been demonstrated. Furthermore, it has been shown that this new technology is a solution to the critical high ambient lighting problem situation, where all other methods have failed. Each aspect of the display system has been shown capable of the required performance, and the next step is a program to simultaneously achieve optimum performance from each of the subcomponent areas. Devices must be fabricated in sufficient numbers and at a sufficient rate to permit parametric control of production through testing and evaluation; liquid crystal material temperature conditioning procedures and new aircraft illumination and viewing configurations must be established for accommodating the special requirements of military systems; and the design must be extended to include larger, higher resolution applications with integrated drive electronics. These achievements will lead to a production base large enough to bring unit costs down to the point where the capabilities of this new display system can be economically utilized in places other than critical applications. The result will be a new generation of display components providing superior performance at competitive cost.

PRESENT STATUS OF CONSTRUCTION AND PROCESSING PROCEDURES

Sufficient experience has been gained in the areas of semiconductor wafer processing and display assembly to permit working liquid crystal displays to be routinely produced. The contruction and testing of over 25 single module displays has led to the identification of the critical steps in the fabrication process, and has provided the necessary feedback to control these steps and improve display performance.

In the area of semiconductor wafer processing, the predominant limit on display performance was due to non-functioning matrix lines that were defective electrically. An investigation into the cause of these defects showed that they came primarily from defects in the masks used to define the electrode structures, and a testing procedure was subsequently developed that allowed these defects to be located, identified, and eliminated.

As a result, it was possible to eliminate all line defects from the matrix array and to demonstrate a defect free single module display.

Similar approaches were also applied in the area of display assembly techniques, where non-uniformities in the display image were caused by flatness variations of the matrix array surface and contamination problems in the liquid crystal material. New measuring techniques were implemented to identify the source of these problems, and as a result new methods were developed for mounting, filling, and sealing the liquid crystal display.

The construction of four quad displays has also been completed. Each of the quad displays is assembled from a precision array composed of four single modules. Consequently, the same technology that was developed for the single module displays was used here, plus the development of new techniques for the final assembly of the modular quad assembly. These techniques included the development of precision wafer sawing methods, accurate positioning and alignment of the modules, special mounting and bonding techniques, and high density connecting schemes. The application of these techniques, resulted in the completion of four quad displays capable of presenting video imagery, and allowed for the subsequent evaluation and testing of display performance. Test results have indicated that the assembly procedures used for the display fabrication gave reproducible results, and that the method of constructing both individual module displays and quad displays is feasible for application to production.

The investigation of interconnection techniques has focused on a wrap-around conductor technique that is applicable to both interconnected and self-contained techniques. A conceptual model has verified the capabilities of this technique, and laid the groundwork for the future construction of multi-module array displays.

Present Status of Display Performance

Discussions of the performance characteristics for single-module displays and quad displays have been presented previously in sections 2 and 6 respectively, and Table 15 summarizes their characteristics. The performance measures were taken under illumination and viewing conditions considered appropriate for a typical cockpit installation, where the pilot is allowed a viewing window of $\pm 15^{\circ}$ in azimuth and $\pm 5^{\circ}$ in elevation.

The display performance indicated in Table 15 is encouraging. Although not fully up to the values that have been demonstrated experimentally the

TABLE 15
PRESENT DISPLAY PERFORMANCE

Display	1" x 1' Single	2" x 2" Quad	Comments
Resolution	100 elem. /in	100 elem. /in	Each linear dimension
Size	1" x 1"	2" x 2"	
Contrast-Max	24/1	19/1	Ideal conditions
Contrast-Min	2.5/1	1.2/1	within viewing window
Reflectivity	50%	50%	of Lambertian
Writing Speed	TV Compatible	TV Compatible	525 line RS170
Response Time	120 ms	120 ms	Decay to 10%
Dynamic Range	8 gray shades	8 gray shades	Ideal conditions
GAP Width	N/A	<1.0 mil	
Defects-Line	0	19	After assembly
Defects-Element	3	17	

numbers are totally consistent with analytic data for the methods employed. Superior construction methods involving smoothing and improved electrode materials were deferred during Phase III, because the major emphasis in the development of the display technology was concentrated on the elimination of the line defects in the electrode array chip. These defects were considered to be the most serious factor affecting the overall display performance and had to be eliminated before a useable display could be built. The achievement of this goal cleared the way toward the production of defect-free displays suitable for aircraft applications. Other display factors, such as brightness and contrast, are already within acceptable levels, and therefore improvement of these factors was given lower priority, although experimental investigations were conducted in parallel in several areas to pursue methods for increasing display performance that could eventually be applied to the basic production processes.

Operating Temperature

The present liquid crystal displays function from +15° to +40°C. The operating temperature range of a liquid crystal material is primarily determined by the number of components one is willing and able to incorporate into a multiple mixture exhibiting eutectic behavior. It is estimated that the -54°C to +71°C range of MIL-E-5272C can be covered with a five-component eutectic mixture. Alternately, the operating temperature range

can be extended by heating and/or cooling the display. (Eutectic mixtures should be storable at temperatures above and below the operating temperature range without damage.) Thus, it appears that the necessary operating temperature range for military applications can be obtained when the basic effort is undertaken.

Display Life

End life or total failure occurs when a device is no longer able to serve its intended role. This exact point is difficult to quantize for a Liquid Crystal Pictorial Display because all evidence points to a "graceful degradation" failure mode, i. e., gradual rather than sudden total catastrophic failure. The only component of the display which is expected to degrade with time is the liquid crystal material. Some of the unneutralized components of the electrochemical reactions that take place at the electrodes gradually reduce the degree of perfection of the liquid crystal molecular alignment, react with other elements in the cell to form unwanted conductivity dopants, and cause the gradual accumulation of small gas bubbles in the display. Quantitative estimates of operational lifetime were obtained by continuously running simple test cells at 20 volts dc and monitoring resistivity. Several of these test cells ran in excess of 15,000 hours before significant changes in the electro-chemical properties were noted. (To eliminate any possible contamination from an alignment technique, no liquid crystal alignment mechanism was provided, and the contrast ratios of the cells was not formally monitored.) The applied potential in an actual display would be considerably less than 20 volts as video signals do not operate continuously at their peak value.

Areas Requiring Further Development

Ultimate use of the liquid crystal display in aircraft applications will require that the display be optimized both for viewing in the intended application and as a mechanical unit to suit specific installation requirements. This will require the use of new processing techniques to enhance display brightness and contrast, increase display size, and develope LSI drive circuits and interconnections to reduce package size and increase reliability. The requirements of the display in each of these areas has already been investigated to determine appropriate methods for improving the display performance. A brief discussion of these requirements is presented below.

Brightness

The brightness of liquid crystal material in its dynamic scattering state is a direct function of the reflectivity of the matrix array electrode-structure. Liquid crystal scattering occurs in the form of a lobe centered around the specular reflection of the incident light off the display surface. The magnitude of this lobe is proportional to the magnitude of the specular reflection, which is determined by the reflectivity of the display electrode surface. Present liquid crystal displays have a reflectivity of only 30 percent, due in part to a relatively low reflectivity value for the metal used to form the array elements. Measurements have indicated that nearly a threefold increase in display brightness realized when superior electrode material depositions are used. Some of these deposition methods are difficult to introduce into the present manufacturing processes. The development of new procedures and techniques for using improved electrode materials will be necessary before displays with increased brightness can be produced on a regular basis.

Contrast

The semiconductor processes used to fabricate the matrix array module consist of oxidation, diffusion, deposition and etching of the wafer surface. The resulting surface of the matrix array therefore exhibits a structure or topology corresponding to the operations that have been performed. The structure affects the optical performance of the display by creating unwanted reflections and dispersion of the incident light. The scattering that results elevates the background or black-level of the display limiting the dynamic range. A significant increase in contrast can be gained by improving the black-level by reducing or eliminating surface irregularities. To make the surface smoother or more mirror-like, a layer can be applied over the display surface to cover-up underlying irregularities and thus provide a good optical surface. The development of such a smoothing layer has been difficult, however, since it must be both thick enough to cover the surface structure and thin enough to be etched for subsequent connections to be made to the underlying electrodes. In addition, it must be compatible with the liquid crystal material to prevent contamination. Several methods have been investigated for creating such a smoothing layer, but further development of manufacturing technology will be required before a workable process can be created.

Size

At the present time, the largest operating liquid crystal television display is a two-inch by two-inch display formed by assembling four one-inch by one-inch chips in a quad array. A prerequisite to the construction of still larger displays is the further development of techniques for assembling chips in a modular mosaic array manner; significantly larger chips are unlikely to be available at a reasonable cost for some time.

LSI Drive and Packaging

The present liquid crystal displays require a large number of electrical circuit connections to drive the display. A practical airborne installation will require that minimal panel space and volume be utilized, if full advantage of the liquid crystal technique is to be taken. The ultimate solution is to use LSI drive circuits mounted around the periphery or to the rear of the active display area. The LSI circuits will interface directly with the matrix array and perform all the necessary multiplexing operations. The need for a large number of display connections will be eliminated, and the space required for the display and drive circuits will be minimized. The use of LSI drive circuits will reduce the liquid crystal display to a single self-contained unit suitable for aircraft panel installations.

ULTIMATE CAPABILITY

The liquid crystal airborne display technology represents the first superior alternative to CRT display systems in terms of performance and ultimately in cost-of-ownership. When in production anticipated capabilities will cover any conceivable cockpit information display application. Table 16 illustrates the likely course of future development assuming continued interest and funding by the government in its pursuit.

RECOMMENDATIONS FOR THE FUTURE

The production of Liquid Crystal Airborne Display systems at a cost that is competitive with present CRT display systems will require a production volume sufficient to achieve reasonable yield and to amortize initial capital investment costs at a reasonable rate. Similarly, the large capital equipment expenditure necessary to achieve this production volume is not going to happen until a market for the display becomes a reality; therein lies

TABLE 16

THE COURSE OF FUTURE DISPLAY DEVELOPMENT

	Today	1976-77	1980	1985
Display Size	2" x 2"	3.5 x 3.5	5.25 x 5.25	7.5 x 10
Number of chips per display	4	4	9	12
Resolution				
Panel displays	200 x 200	450 x 450	670 x 670	960 x 1300
Head-up or magnified displays (3.5" x 3.5")	N/A	450 x 450	890 x 890	2000 x 2000
Contrast	15:1	30:1	45:1	45:1
Reflectivity/ Brightness (Percent of Lambertian)	50%	100%	200%	200%
Temperature	Room temperature	Extended low temperature	Full Mil Spec	Full Mil Spec
Color	Experimental	Developmental	220 line, full-color television	320V x 430H full-color television

"Catch 22" and as with many new technologies, liquid crystal display is at the point where now that feasibility is proven, it awaits a user with a program whose timing and needs match what is possible to achieve in a modest beginning production effort.

APPENDIX A
DISPLAY REQUIREMENTS

Single-place, all weather attack aircraft of the future will require highly reliable multifunction displays for flight control, sensor display, navigation, aircraft systems monitoring, threat warning and armament control functions. If the pilot is to effectively control operation of the aircraft and its weapon system, these displays must be optimized to provide an effective means of monitoring automatic functions and to present data needed for the semi-automatic and manual control of system functions.

Existing aircraft using CRT display technology either have limited visibility during daylight operations because of reduced display contrast, or they have reduced CRT lifetimes because of the higher device performance demanded to counteract the very high ambient illumination. With the trend toward greater visibility of the outside world, which implies even higher luminance values, new display technology must be developed. This section is directed toward applying the liquid crystal display to those airborne applications where the existing technology is incapable of satisfying brightness and contrast requirements.

SENSORS AND PERFORMANCE

Mission requirements dictate the use of a system approach in designing avionics and weapon systems displays and controls. The goal should be a display subsystem that presents only essential information in a format that permits it to be easily assimiliated by the pilot for translation into direct control inputs. Many of the pilot's routine and repetitive tasks suggest automation and some degree of computer aided decision making as a means of alleviating his work load. For the liquid crystal display, a basic avionics design concept and baseline system capabilities, will be defined in terms of display device requirements. Essential to this definition, are the sensors utilized for target acquisition and designation, cautionary information (radar homing and warning, and etc.), and the extension of pilot range of visibility during night or adverse weather operations.

Sensor display requirements have the largest impact on display system mechanization. This is because of the high resolution and large dynamic range required for presenting pictorial imagery as opposed to symbolic data. Also, radar sensors and some FLIR sensors require intermediate storage and scan conversion if they are to be displayed in a raster scan format irrespective of whether or not they use CRT or liquid crystal components. The basic requirements in terms of resolution and input/output rates are determined from an analysis of a multi-mode radar, two types of FLIRS, and various television sensors.

A summary of the major parameters of the proposed sensors projected for the 1980 era and the implications of these parameters for display system design are given in Table A-1.

DISPLAY AND SYMBOL REQUIREMENTS

The pertinent avionics display applications for liquid crystal include: an advanced Head Up Display (HUD), a multisensor Vertical Situation Display (VSD), and a Master Monitor Display (MMD). Present state of the art and reliability considerations dictate that a digital scan converter and a symbol generator be an integral part of these display systems.

Suggestions for future implementations of the liquid crystal approach require the stated assumptions by individual display type (HUD, VSD, and

TABLE A-1
SENSOR DISPLAY REQUIREMENTS

Sensor	Format	Resolution	Shades of Gray	Update Rate, Hz
Radar				
Real Beam Ground Map	PPI	600 x 225	7	0.5
DBS Ground Map	PPI	600 x 520	7	0.25
FLIR	TV Type Raster	480 x 600	10	30
LLLTV	TV Raster	800 x 800	10	30
Missile TV	TV Raster	490 x 450	8	30

Stop

IR.C 22

MMD) in which the symbology and display requirements for each is stated as appropriate.

Head-Up Display (HUD)

Table A-2 indicates that a HUD designed to take full advantage of the entire operational envelope provided by future weapons and sensors should provide a field-of-view of ±30 degrees in azimuth and +15 to -22 degrees in elevation. The FOV requirements although satisfying operational needs, are not necessarily compatible with installation requirements. It is unlikely that an elevation field-of-view of +15 to -22 degrees would fit in a fighter cockpit and ±30 degrees although relizable with the windscreen boundaries, is not achievable by any optics method presently known. In Table A-3, realistic goals for advanced HUDs are set forth.

For the near-term, aricraft such as F-16, and etc. would require liquid crystal displays to satisfy the goals of Table A-4.

TABLE A-2

HUD FIELDS OF VIEW - BASED UPON FUTURE OPERATIONAL REQUIREMENTS

Source of Requirement	Azimuth	Elevation
Landing	±15 degrees	+5 degrees, -22 degrees (over the nose) (A-10 aircraft)
Trainable guns	±30 degrees	—
Fixed guns	±5 degrees	+4 degrees, -8 degrees
Bombs	±10 degrees	-22 degrees (over the nose)
Sensor video	±10 to 15 degrees present ±30 degrees future	±10 degrees ±15 degrees future
Flight-control	±30 degrees	

TABLE A-3

ADVANCED HEAD-UP DISPLAY DESIGN GOALS
FOR FUTURE AIRCRAFT

Field of View	
Horizontal	30 degrees
Vertical	25 degrees
Brightness/Contrast	Provide contrast ratio of 1.8:1 with 110,000 lux (10,000 ft-c) ambient
Transmission	Maximize (no less than 80%)
Resolution/Accuracy	Maintain 1 mrad over central field-of-view
Refresh Rate	60 Hz minimum (data update rate 25 Hz min.)
Color	Yellow-gree (5432Å) or others such as red for night operations, and etc.

TABLE A-4

NEAR-TERM HEAD-UP DISPLAY DESIGN GOALS

Field of View	25 degrees circular
Brightness/Contrast	Contrast ratio of 1.2:1 min. against 10 kfL background
Transmission	80% or greater transmission for pilot's forward view
Refresh Rate	60 Hz min.
Data Update	25 Hz min.
Color	Yellow-green (5432Å) or other monochromatic values in the region of photopic eye response

Vertical Situation Display (VSD)

The Vertical Situation Display (VSD) is a primary flight and sensor data display system that presents both flight control data and sensor data for navigation and weapon delivery. In this role, the VSD provides integrated presentations of essential data required in the flight control of the aircraft. These include: attitude, velocity, altitude, heading, angle of attack, vertical velocity and command data. As one of the primary sensor displays, the

VSD must accommodate whatever sensors may be on-board the aircrait. These will include multi-mode radar forward looking infrared (FLIR); low light level television (LLLTV); and TV guided weapons. Therefore, the VSD must be compatible with a wide variety of data input for mats and data rates. These requirements indicate a need for scan conversion and reformatting of data.

Use of the VSD as the primary flight data display, requires the integration of individual flight data elements into a presentation which is readily and accurately interpreted by the pilot. Representative VSD parameters appear in Table A-5.

Master Monitor Display (MMD)

A summary of the recommended Master Monitor Display parameters, determined from previous studies at Hughes, is presented in Table A-6.

The display parameters of brightness, contrast viewing angle, and resolution are similar to those for the VSD. They are discussed in the following section: "Human Operator Requirements."

HUMAN OPERATOR REQUIREMENTS

The human operator requirement can be categorized into the psychophysical attributes of human vision important to liquid crystal display design for the HUD, VSD, and MMD designs. The categories are listed in the following

- Viewing Environment – Ambient Illumination
- Modulation Sensitivity Function of Human Vision
- Gray Levels and Dynamic Range
- Temporal Factors

TABLE A-5
VSD PARAMETERS

Display Size	15 x 15 cm (6 x 6 in.)
Viewing Distance	71 cm (28 in.)
Viewing Angle	12°

Stop

TABLE A-6

RECOMMENDED ALPHANUMERIC/DISPLAY PARAMETERS*

Symbol Style	Leroy
Symbol Height	0.24 inch
Symbol Spacing	1 stroke width between characters 1 character width between words
Symbol Width to Height Ratio	0.80 for characters 0.70 for numerals except "1" 1 stroke width for numeral "1"
Stroke Width to Height Ratio	1:7.5
Line Spacing	0.24 inch
Contrast Ratio	2:1 (minimum)
Refresh Rate	60 Hz
Update Period	Not less than 1/4 second for single parameters
Delay in Response to Input	Not more than 1 second
Display Size	5" x 7" usable area

*Assumes a viewing distance of 28 inches and a maximum ambient brightness of 110,000 lux (10,000 ft-C).

Viewing Environment

A primary consideration governing liquid crystal display design is the viewing environment. In modern aircraft, the salient factors are the ambient illumination, the viewing distance, and the cockpit geometry. Representative ambient illumination levels are summarized in Table A-7. Viewing distances and angles of regard must be determined from the specific aircraft intended for the application. Viewing distances typically range from 20 inches for the vigilant eye to 30 inches for the task eye in most single-place aircraft.

Operator/Psychophysical Evaluation Criteria

The modulation sensitivity function (MSF) of human vision describes the capability of the operator to resolve spatial frequencies as a function of intensity modulation and average display luminance. To obtain the MSF, a pattern of sinusoidally modulated lines is presented to the observer and either the modulation or the spatial frequency is varied.

The MSF curves shown in Figure A-1 imply a spatial frequency cutoff in the region of 40 cycles per degree. This says that the limit of visual acuity

TABLE A-7

AMBIENT ILLUMINATION

Illumination Condition	Level, Foot Candles
Direct Sunlight	11,000
Clear Sky	2,000
Average Cloud Cover	7,000
Deep Twilight	1×10^{-1}
Full Moon Clear Sky	2×10^{-2}
Quarter Moon Clear Sky	1×10^{-3}
Starlight	1×10^{-4}

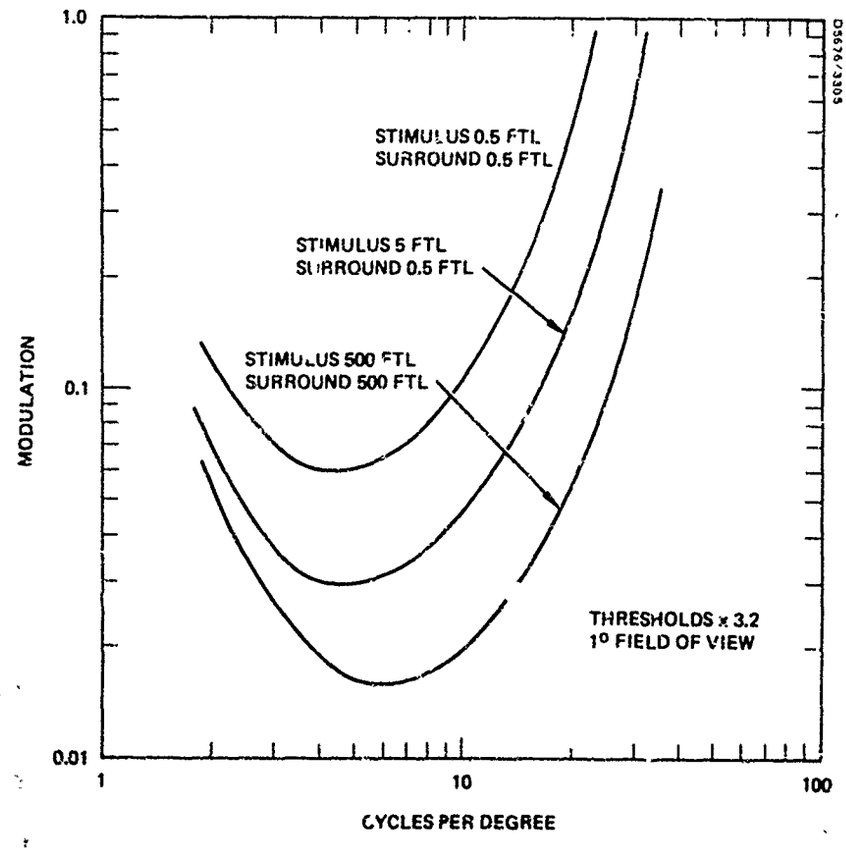


Figure A-1. Observer sine-wave modulation demand function.

is on the order of 0.75 arc-minutes. It is well known, however, that long lines of high contrast, say telephone wires against the sky, can be seen when the line width subtends only a few seconds of arc. This special case is of interest in display images formed by matrix displays where the inactive display area between picture elements may be visible. This is especially true in LED or in fibre optic arrays where small matrices may be butted and joined together to form a large matrix. The butting joint may form a relatively long inactive line sharply defined because of its high contrast. Such lines may be visible under conditions not predicted by the MSF data. A graph illustrating the visibility of lines — modulation not stated — is shown in Figure A-2. At high illumination, such lines can be seen when they subtend less than one-second of arc. The width of the line that can be seen at 30 inches viewing distance is shown on the ordinate.

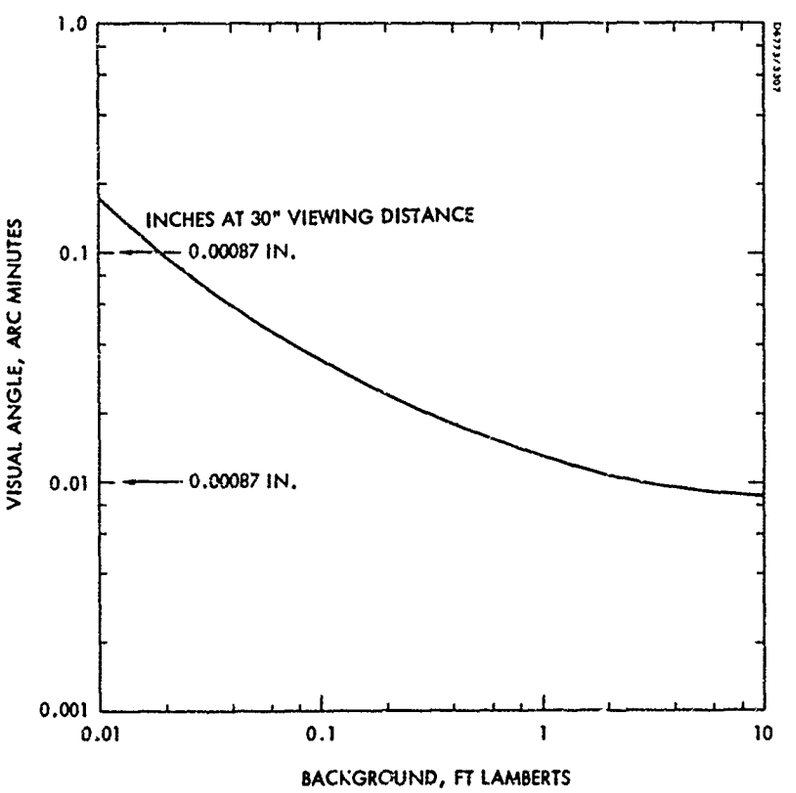


Figure A-2. The relation between brightness of background and visual angle subtended by thickness of line when it just becomes resolved against the illuminated background.

Gray Levels and Dynamic Range

The total dynamic range of vision is enormous if one considers the disparity between the luminance of snow in the sun to the luminance of dark sand in faint starlight. As can be seen from Figure A-3, the eye can respond to luminances as high as 16, 000 mL before human tolerance is exceeded and as low as 0. 000001 mL before the luminance energy level becomes too low. This figure also demonstrates that human vision is a "dual" system; where the photopic system is appropriate for daylight observation and the scotopic is used at night. Because of the low acuity of scotopic vision the use of displays driven at low luminance levels is inappropriate for the extraction of

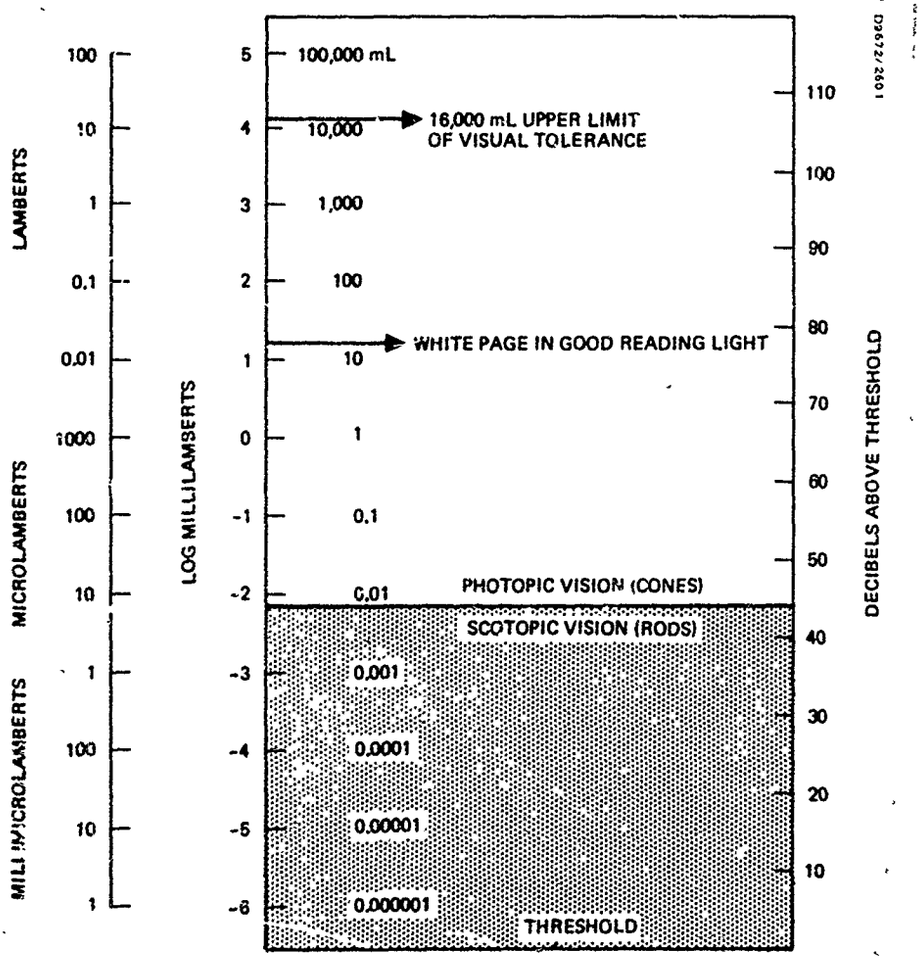


Figure A-3. Range of light intensities that the human eye confronts(A-1).

(A-1) Stevens, S.S., Handbook of Experimental Psychology, 1951, John Wiley and Sons, New York.

detailed information. The region of interest to the displays designer is photopic vision in which the total dynamic range exceeds 1 million to 1. However, the instantaneous dynamic range is considerably less; on the order of 100:1 to 500:1, providing a window or range of luminances whose absolute value is controlled by the visual adaptation level. If the eye, for example, is adapted to 1000 fL, then any luminance below 2 fL will appear black and no luminance discriminations can be made below that level.

To estimate how much intensity information can be communicated by a display, one must consider the luminous range of the image – in the limit case the instantaneous visual dynamic range – and the differential brightness threshold; the amount by which a base level luminance must be raised to assume that an adjacent luminance will appear as a brightness difference to an observer. The MSF data informs us of the modulation required to discriminate two grey levels as a function of spatial frequency and adaptation level. The total number of discriminable grey levels for a given spatial frequency is a function of the modulation demand at that frequency and the dynamic range at that frequency. An estimate is provided by:

$$X = \frac{\log Z}{\log \left(1 + \frac{2M}{1 - M}\right)} + 1$$

where:

X = number of discriminable grey levels

Z = dynamic range $\frac{B_{max}}{B_{min}}$

M = demand modulation

Calculations have been made using this formulation over a range of dynamic ranges, spatial frequencies, and adaptation levels. Account was taken in the computation of the "adaptation mismatch" caused by the large dynamic-range inherent in the display itself. The results are plotted in the graphs of figures A-4, A-5, and A-6 for day, dusk, and night conditions, respectively. The "day" graph, for example, shows that 50 grey levels can be discriminated at a spatial frequency of 16 cycles per degree when the display dynamic range exceeds 100:1. At 10:1 dynamic range about 32 grey levels can be discriminated.

Stop

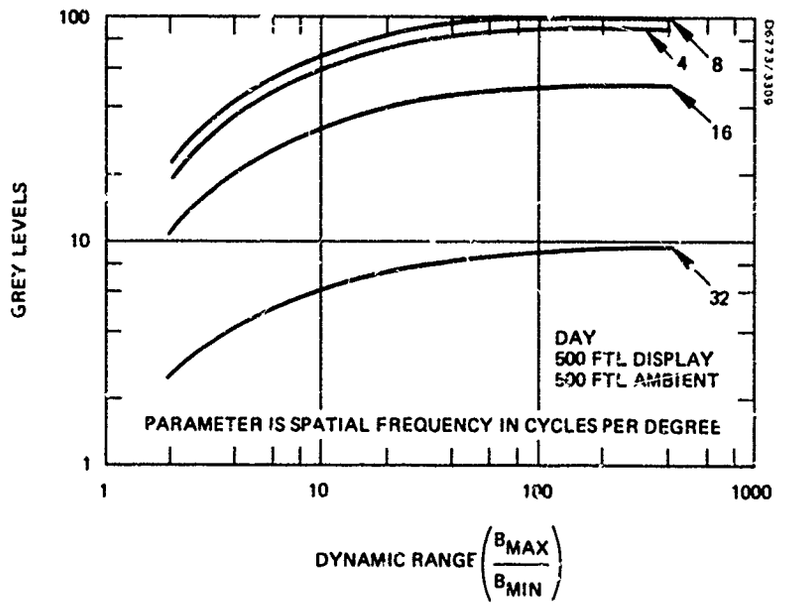


Figure A-4. Discriminable grey levels as a function of dynamic range and spatial frequency — day.

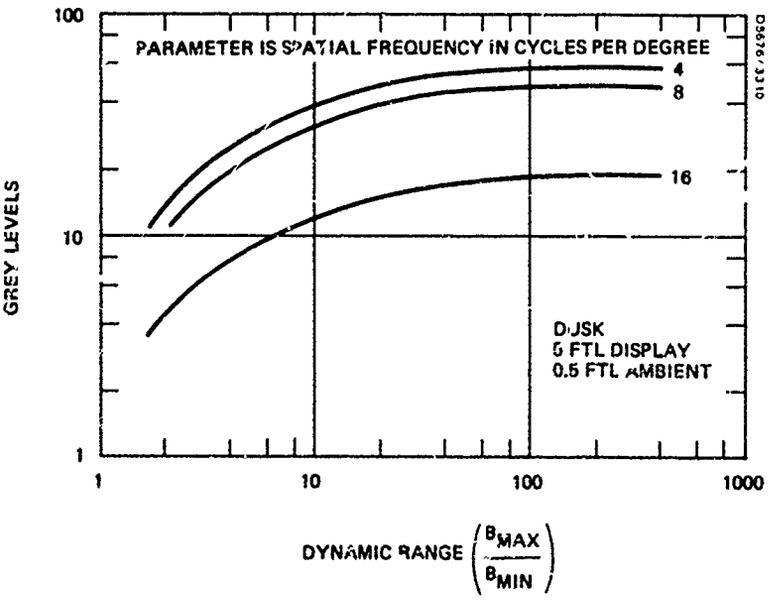


Figure A-5. Discriminable grey levels as a function of dynamic range and spatial frequency — dusk.

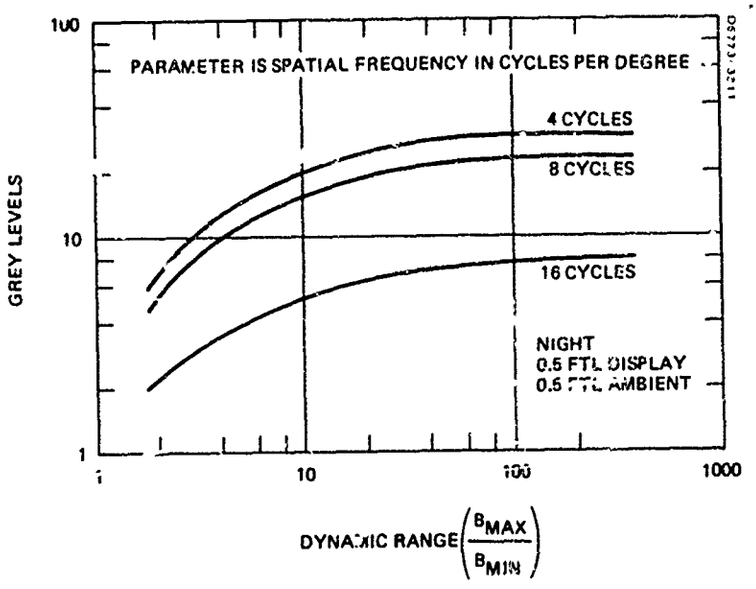


Figure A-6. Discriminable grey levels as a function of dynamic range and spatial frequency — night.

One may estimate a generalized figure of merit for grey level capability of displays by normalizing the discernible grey levels to a dynamic range of 400:1 (the asymptote of vision) and expressing the merit of other dynamic ranges as a percentage of the maximum theoretical number of discernible grey levels. The results of such an exercise are shown in Figure A-7.

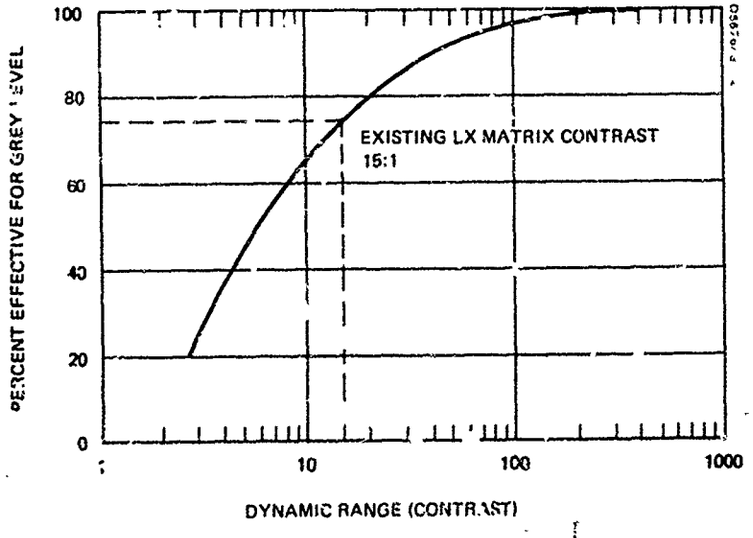


Figure A-7. Grey level figure of merit as a function of dynamic range.

This is a first approximation based on an involved extrapolation and should be treated as such. It indicates, however, that existing matrix contrast is satisfactory and that with ell smoothing, display figure-of-merit should exceed 90 percent.

Temporal Factors

The design of displays must account for two temporal factors that affect the appearance and utility of the display; the refresh rate and the information update rate. The refresh rate determines whether or not the display will flicker. Conventional TV rates of 60 Hz (30 frames with 2:1 interlace) were selected to obviate flicker when the average television display luminance was suitable for room illumination. Kelly, 1961[A-2] conducted flicker threshold studies using sinusoidal modulation of the stimulus luminance over a broad range of display luminance. Partial typical results for one observer are plotted in Figure A-8. Kelly synthesized his and other data to provide the more general curves illustrated in Figure A-9. These curves indicate that, to be flicker free, displays driven at high luminance, say 500 fL and high temporal modulation (<0.5) will require refresh rates on the order of 70 Hz.

In motion pictures, television, and other sampled data displays the displayed image is physically stationary. The successive displacement of information images over several frames yields apparent motion. A comprehensive discussion of the psychophysical conditions that yield the impression of motion is beyond the scope of this discussion. Among undesirable phenomenon that occur with intermittently updated displays is the appearance of multiple images. Multiple images have been observed on both LED and CRT displays that are updated periodically when the imaged information is moved between updates such that successive pictures stimulate different regions of the retina. This can occur because of displacement of the observer, displacement of the entire display, or displacement of the information; in fact, any motion that yields displacement of the image on the retina between successive updates.

[A-2] Kelley, D. H., Visual response to time-dependent stimuli. I. Amplitude sensitivity measurements. Journal of the Optical Society of America, 1961, 51, 422-429.

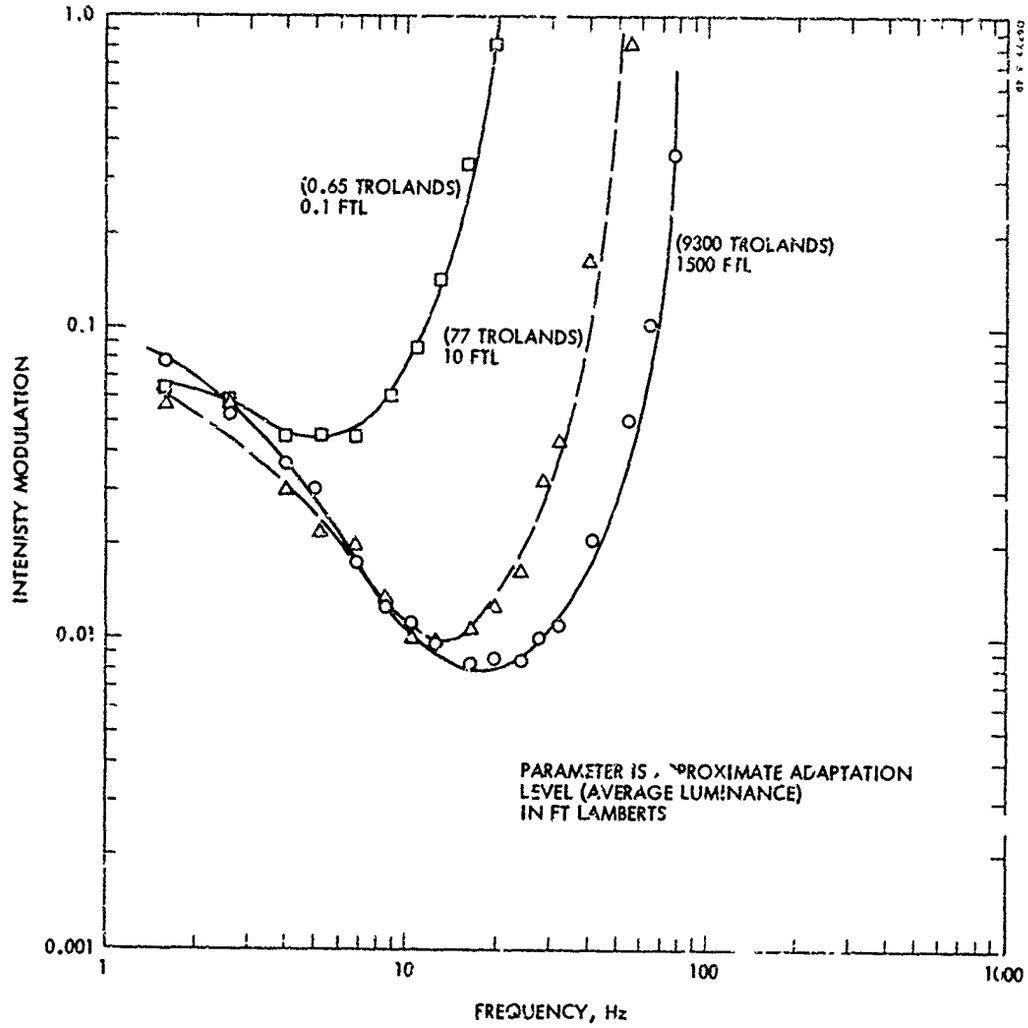


Figure A-8. Flicker fusion thresholds as a function of modulation level, adaptation level, and frequency of sinusoidal modulation(A-2).

One can account for this phenomenon with a single assumption; that the integration interval for vision is longer than the interval between successive updates. The precise value for visual integration is not well established but it has been frequently observed that intermittent visual events occurring within 100 milliseconds will appear to happen simultaneously. Given the assumption of a 100 msec visual integration period, multiple images will

(A-2) Kelley, D. H., Visual Responses to time-dependent stimuli. I. Amplitude sensitivity measurements. Journal of the Optical Society of America, 1961, 51, 422-429.

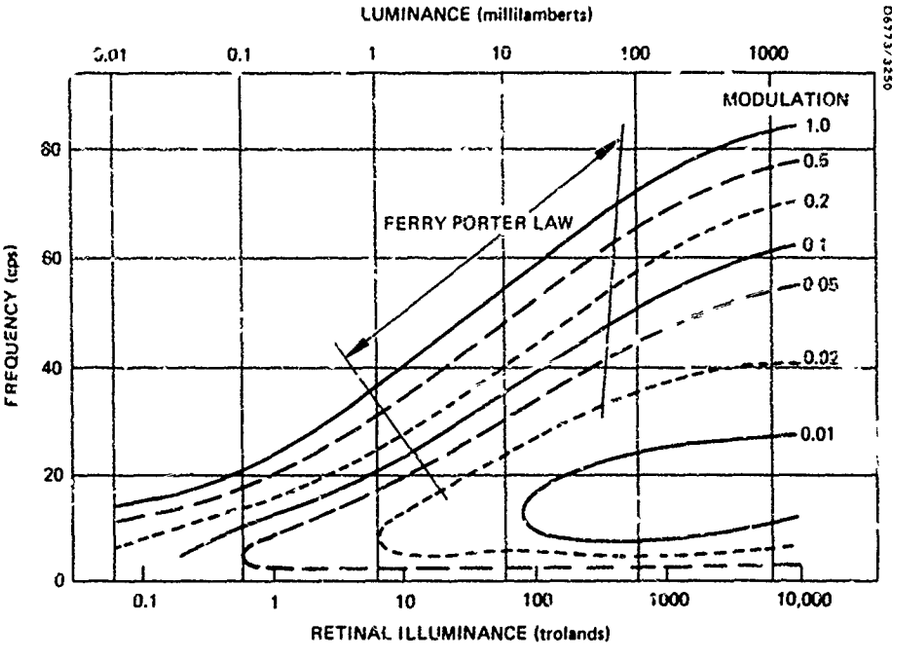


Figure A-9. Threshold frequency versus adaptation level as a function of modulation(A-1)

appear when successive displacements of intermittent images exceed the visual acuity threshold within an interval of 100 msec. Thus a spot updated at a rate of 100 Hz, displaced between updates a distance of 2 arc-minutes will yield multiple images; i. e., in 100 msec, ten spots separated by 2 arc-minutes will be seen as occurring simultaneously.

A graph illustrating this relationship for three possible acuity thresholds and one integration interval (100 msec) is provided in Figure A-10. For convenience the ordinate has been labelled as though the image were moving. Thus assuming a one arc-minute acuity limit, and an update rate of 60 Hz, the boundary for multiple images will be motion of 6 arc-minutes per second. Slower update rates or image motion should be free of multiple images.

In conclusion, the important psychophysical measures presented in this section will be applied to the determination of display size, pixel density, and total resolution required for the liquid crystal display for HUD, VSD, and MMD applications.

(A-1) Stevens, S. S., Handbook of Experimental Psychology, 1951, John Wiley and Sons, New York.

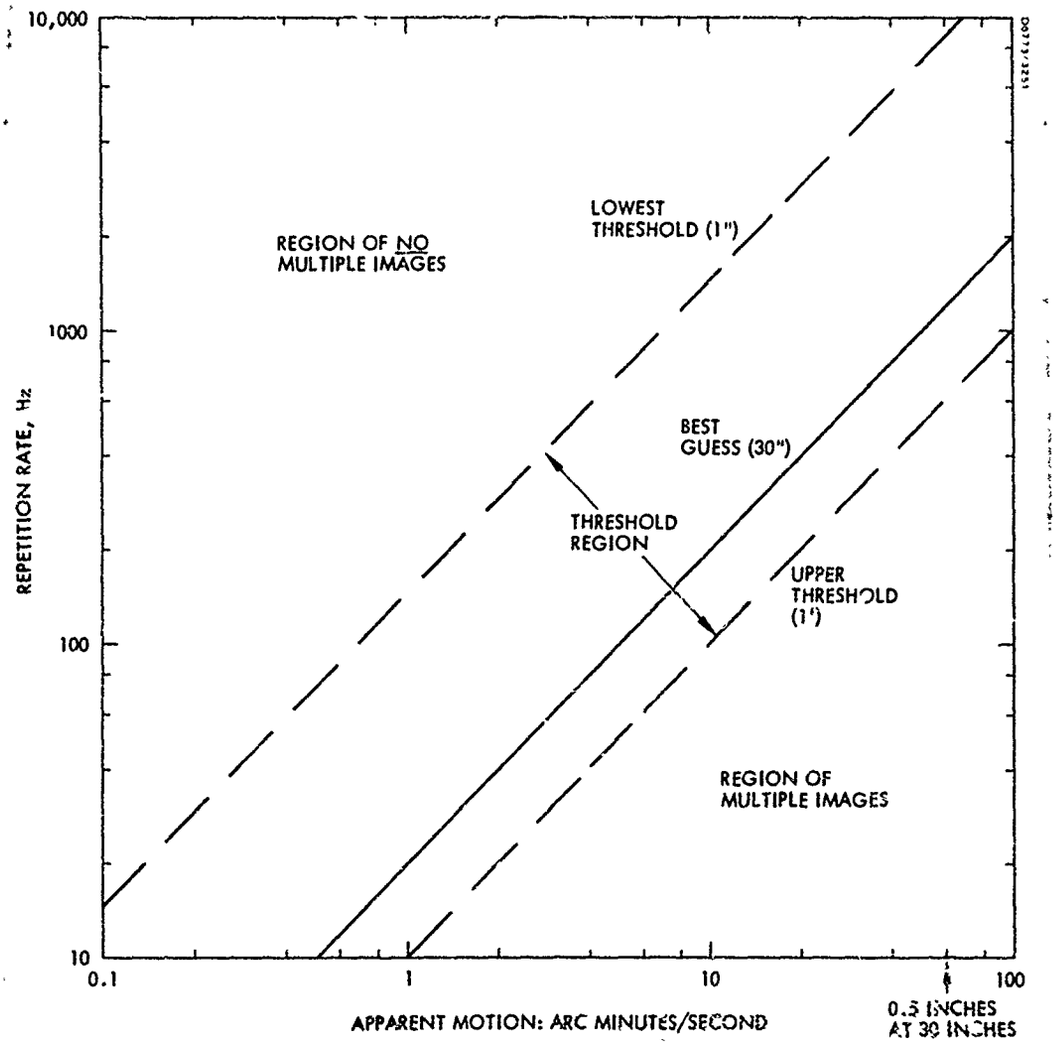


Figure A-10. Conditions for multiple images in LED and other updated type displays.

MATRIX DISPLAY REQUIREMENTS

Based upon the foregoing discussion of the display information content and the human operator requirement for viewing it, the matrix requirement for picture element density and total resolution will now be developed for the HUD, VSD, and MMD avionics applications.

HUD Criteria

Although the visibility of HUD symbols depends on brightness and contrast, the legibility of alphanumeric characters depends on symbol size, stroke width, as well as system resolution. Figure A-11 illustrates the

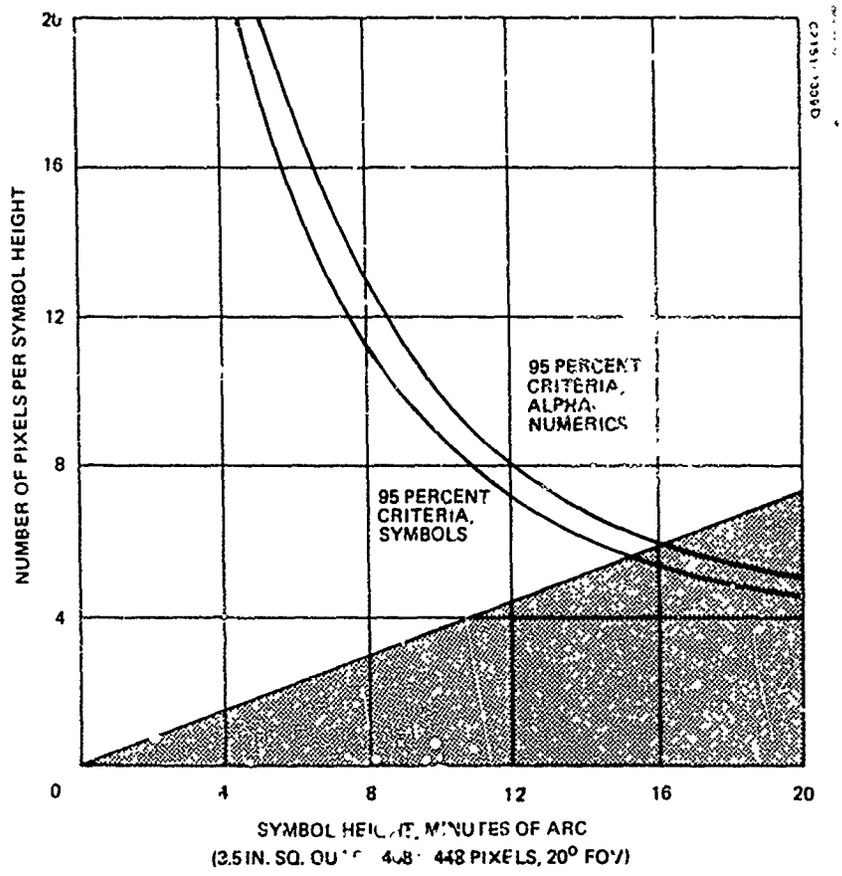


Figure A-11. Criteria for 25° FOV, HUD with matrix display of alphanumerics and symbols.

interaction between alphanumeric symbol size and resolution with a criterion curve drawn at the loci where the alphanumerics will be correctly identified 95 percent of the time. This criterion curve was derived from laboratory data for high contrast symbols[A-3, A-4, and A-5]. Alphanumeric legibility is also a function of the ratio of stroke width to symbol height. Acceptable ratios[6] are on the order of from 1:5 to 1:8.

[A-3] Erickson, D. A., and Hemingway, J. C., Image Identification on Television. Naval Weapons Center, China Lake, 1970.

[A-4] Shurtleff, D., Design Problems in Visual Displays – Part I, Classical Factors in the Legibility of Numbers and Capital Letters, Mitre Corp., 1966.

[A-5] Shurtleff, D., Design Problems in Visual Displays – Part II, Factors in the Legibility of Televised Displays, Mitre Corp., 1966.

Referring to Figure A-11, the criterion of 90 percent gibility is more critical for alphanumerics than it is for symbols. The shaded area of Figure A-11 represents application of a liquid crystal quad matrix to a HUD with a 20° total field-of-view. This design represents existing technology that is available now and can be applied to display production in the 1977-1978 time period. A 1.75 inch square display can be fabricated within a 3 inch substrate, allowing for edges and handling. It is also assumed that in fabricating new masks required for 3 inch production, that a resolution of 128 pixels per inch will be utilized. This results in the completed quad containing a matrix array of 448 x 448 pixels within a 3.50 inch square.

Figure A-11 ndicates that the minimum allowable symbol height for a 20° total field-of-view HUD is approximately 16 minutes of arc for the 448 x 448 matrix. These data cannot be taken as sole criteria for HUD displays, however, as the following discussion will indicate.

Although legible, assililation of information from a HUD comprised entirely of minimum sized characters would not necessarily be rapid because of the mitigating effects of simultaneously performing in-flight operations while viewing moving display imagery against objects in the real-world scene, which are also changing dynamically with respect to the aircraft.

Utilizing increasingly larger alphanumerics improves assimilation but under the penalty of increased obsecuration of the real-world image by the symbolic structure of the display virtual image. The display clutter begins to be significant if the alphanumeric size is increased beyond approximately 35 minutes of arc. A subjective analysis conducted at Hughes[7] has indicated that for an easy-to-read 21 degree field-of-view HUD presentation, the alphanumeric size should be at least 20 minutes of arc in the vertical dimension but should also be less than 30 minutes of arc to provide a minimum clutter presentation.

The analysis thus far has been for the upright presentation of symbols and alphanumerics. Other studies conducted at Hughes[A-6] concerning the legibility of symbolic and alphanumeric characters formed by dot matrices indicate that a 5 x 7 array of dots while entirely adequate for the presentation of upright characters, is not all satisfactory for rotated ones (see Figure A-12). Assimilation time increases and legibility decreases proportionally.

[A-6] Vanderkolk, R. J., Herman, J. A., and Hershberger, M. L., Dot Matrix Symbology Study, HAC Ref: D1165, March 1975.

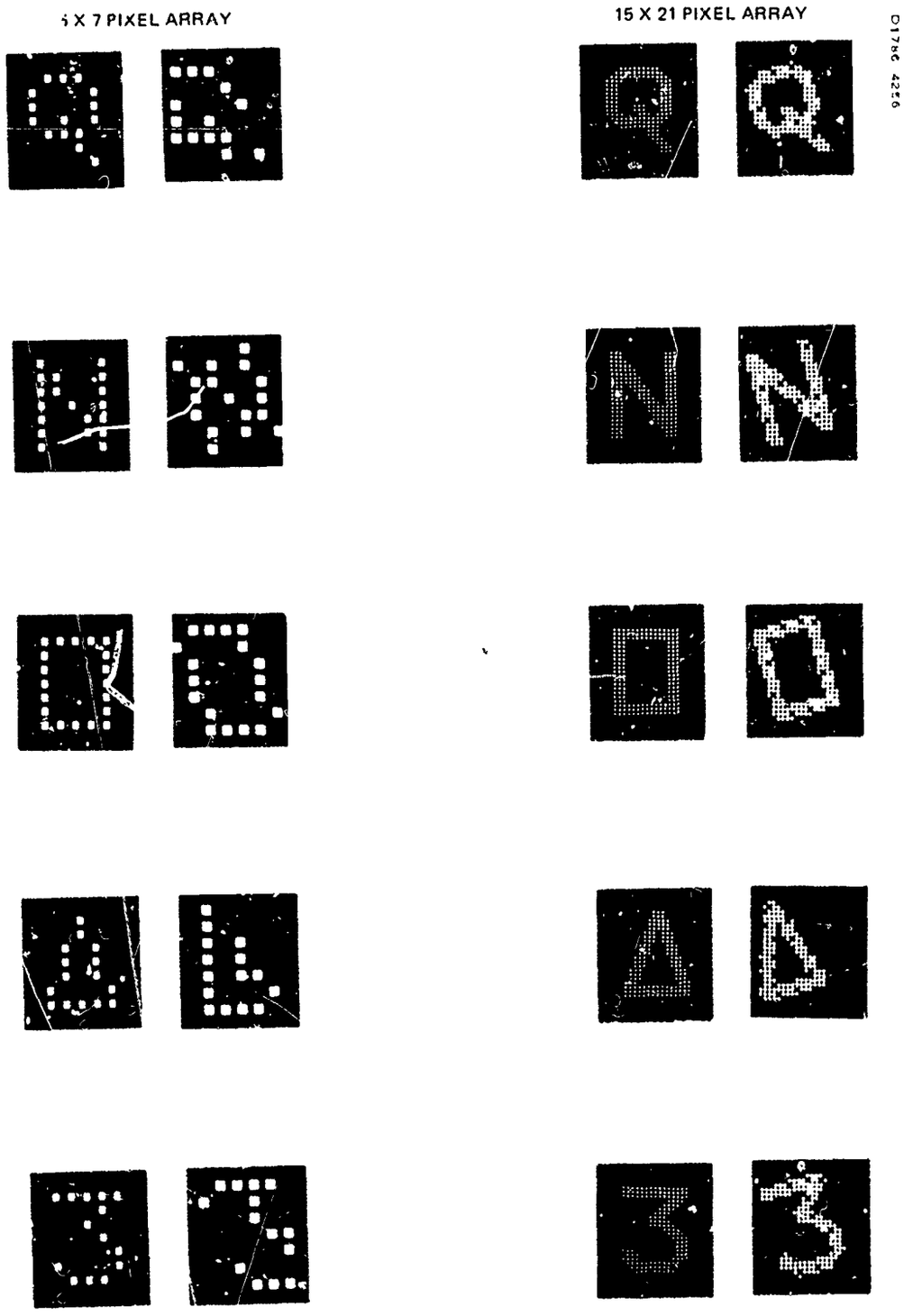


Figure A-12. Comparison of 15 x 21 pixel array to a 5 x 7 array.

The same study has also shown that although a rotated 8 x 11 format is equivalent in terms of recognition time and legibility to an upright 5 x 7 matrix, its appearance is quite poor due to the displacement of linear character edges by the matrix structure. The recommended structure for optimum assimilation and esthetic appearance is the 15 x 21 matrix presented in the right-hand half of Figure A-12.

Granularity, or the number of pixels per degree is dependent upon the following:

- Character height
- HUD system accuracy (maximum permissable boresight error)
- Desired stroke width-to-height ratio (1:5 to 1:8)

The minimum character height was determined earlier to be 16 minutes of arc, but in the interest of improving assimilation while not obscuring the real world, a value of 30 minutes of arc (8.7 milliradians) has been chosen for the alphanumeric character height. Using this value, the required vertical spacing of the pixels for a 15 x 21 dot matrix font is 1.4 minutes of arc (0.4 milliradians).

The USAF specification for HUD accuracy states that display deviation from boresight over the central FOV cannot exceed 1 mrad, so HUD system accuracy is also satisfied by the 0.4 mrad criteria. Applying the 1:8 and 1:5 rule discussed earlier, symbol stroke-to-height width should be between 3.75 to 6 minutes of arc or between 1 to 1.75 mrads, yielding from 3 to 4 pixels per stroke width.

In conclusion, a pixel size of 0.4 mrad will satisfy human operator requirements for legibility and comprehension as well as for system accuracy.

Now that the criterion of 0.4 mrad has been established, the total number of resolution elements per HUD field-of-view can be stated. For the 20° total FOV HUD, this yields a matrix display of 875 x 875, or 766 thousand pixels total resolution over the field-of-view (i.e.: 44 pixels per degree FOV).

Utilizing the same criteria and working under the assumption that the 448 x 448 liquid crystal matrix would be the most likely near-term (1977-78) display component available for HUD application, it can be seen that the total field-of-view should be restricted to 10 degrees.

The foregoing analysis is conservative in that it presents the requirements for optimum legibility, assimilation, and etc. More important, it is based upon rotating symbology. If the symbols remain upright during flight wider fields-of-view can be accommodated. Finally, the resolution/granularity that is recommended can best be determined from simulator and flight test evaluation using symbol generator techniques that provide the flexibility to parametrically vary character height, degree of rotation and pixel height.

VSD Criteria

The data from the previous discussion have been reformatted for VSD alphanumerics in Figure A-13. The basic requirements are summarized in Table A-8.

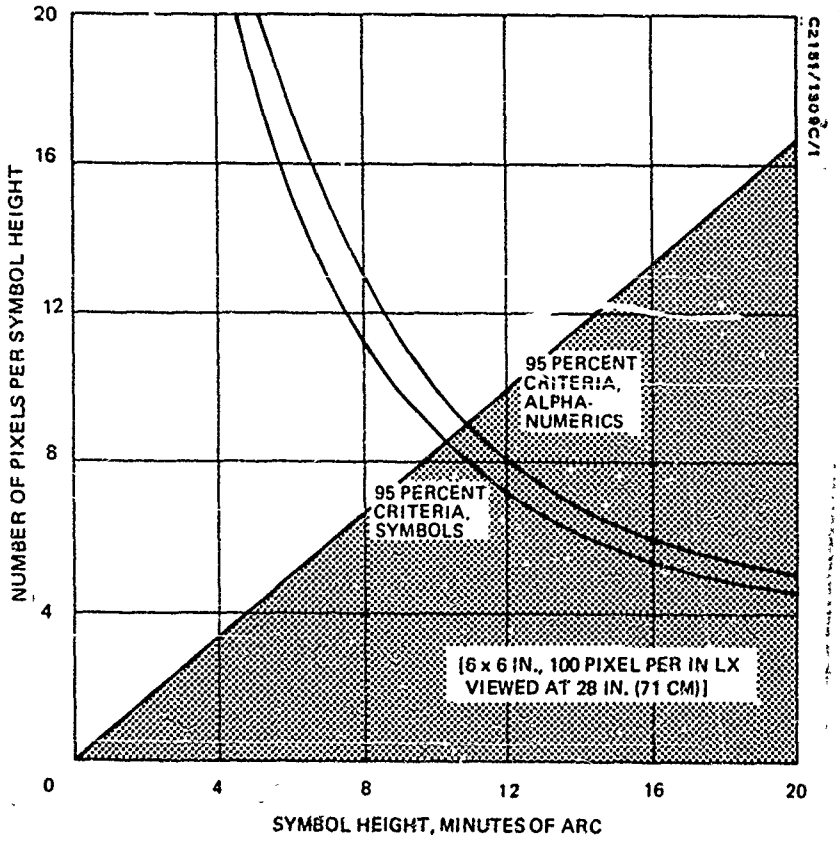


Figure A-13. Criteria for VSD alphanumerics and symbols.

TABLE A-8

VSD MATRIX REQUIREMENTS FOR 15 x 15 cm (6 x 6 in) PANEL DISPLAY

Variable	Requirement
Symbol Height	16 Minutes of Arc, Minimum (This corresponds to 3.3 mm (0.13 in.) symbol height at 71 cm (28 in.) viewing distance.) 27 Minutes of Arc Recommended if Symbol is Subject to Blurring, i.e., of low contrast or unfavorable width-to-weight ratio.
Symbol Width-to-Height Ratio	0.5 to 1.0
Symbol Stroke Width-to-Height Ratio	1:8 to 1:5 — (This variable has a minor effect on symbol legibility.)

Similarly, these criteria apply to the MMD panel when raster-formed symbology is used. An independent study[A-7] conducted at Hughes has indicated that for stroke symbology, character heights ranging from 0.3 cm to 0.6 cm (14 to 31 min. of arc) result in good comprehension. A conservative recommendation for the MMD is to use a 30 min of arc character height with 30 min spacing for line justified raster-scanned characters.

In summary, it is important to note that the various criteria that have been applied throughout this analysis to the determination of resolution density are consistent with one another when expressed in pixels per degree. Table A-9 summarizes this. Since the recommendations for resolution density are based chiefly upon the recognition and comprehension of high contrast alphanumerics, they will remain valid only if recommended values of display brightness and contrast can be maintained. The following analysis sets forth the requirements.

(A-7) Naval Air Development Center, Master Monitor Display Study, Final Report No. P73-464, Contract No. N62269-73-C-0138, Hughes Aircraft Company, Culver City, California, January 1974.

TABLE A-9

CRITERIA FOR DETERMINING PIXEL STRUCTURE/
RESOLUTION DENSITY

Item	Value (Pixels Per Degree)
Acceptable Granularity for Panel Display Matrix Structure viewed between 50 and 71 cm	36
95% Legibility of alphanumerics and symbols (static viewing)	14 to 240
HUD	
Recommended Granularity using 30 min arc alphanumerics comprised of 15 x 21 pixel matrix = 0.4 mrad per pixel	44
VSD	
Recommended Height for 15 x 21 pixel Symbol viewed on 15 x 15 cm VSD at 71 cm = 27 min of arc	47
MMD	
Recommended alphanumeric character height for an MMD viewed at 71 cm = 30 min. of arc. (15 x 21 character)	42

APPENDIX B
SEMICONDUCTOR FABRICATION PROCESSES

The bulk of the work in assembling a liquid crystal matrix display is in producing the semiconductor chip which contains the matrix of circuits for addressing each picture element (optically reflective electrodes), over which a thin-film of liquid crystal is eventually deposited. The required semiconductor processing encompasses those procedures which form the matrix array of transistors, capacitors, and electrodes within and upon the surface of the silicon wafers. Among the processing procedures included are masking, etching, doping and thin-film depositions for conductors and insulators.

Masking is a high-resolution photolithography operation and is used to define the regions on the wafer where a subsequent etch, deposition, or diffusion will affect the surface. The three basic steps that make up a masking operation are shown functionally in Figure B-1. In practice, they are quite involved and carefully controlled. During processing, these steps will be repeated many times. First, a light-sensitive photoresist is applied in a manner that will cover the wafer evenly with a thin coat of the material. Spinning is the traditional technique used for semiconductor wafers, as the thickness of the photoresist can be precisely controlled by monitoring the viscosity of the solution and the speed at which it is spun on (see Figure B-1a). Secondly, the wafer is exposed by a mask as shown in Figure B-1b. If positive photoresist is being exposed, its polymerization will be destroyed by the ultraviolet light. With negative photoresist, the polymerization is stabilized by light. The photoresist is exposed by projection printing for the liquid-crystal display project because it minimizes mask damage. Lastly, the photoresist is developed as shown in Figure B-1c. Rather than being simply dipped in a solution as illustrated, about 20 wafers at a time are placed in a teflon tray, automatically dipped in the appropriate chemicals and washed. These steps are repeated several times in processing sequences which form the multiple layers and diffusions that result in the desired electrical circuit elements and characteristics.

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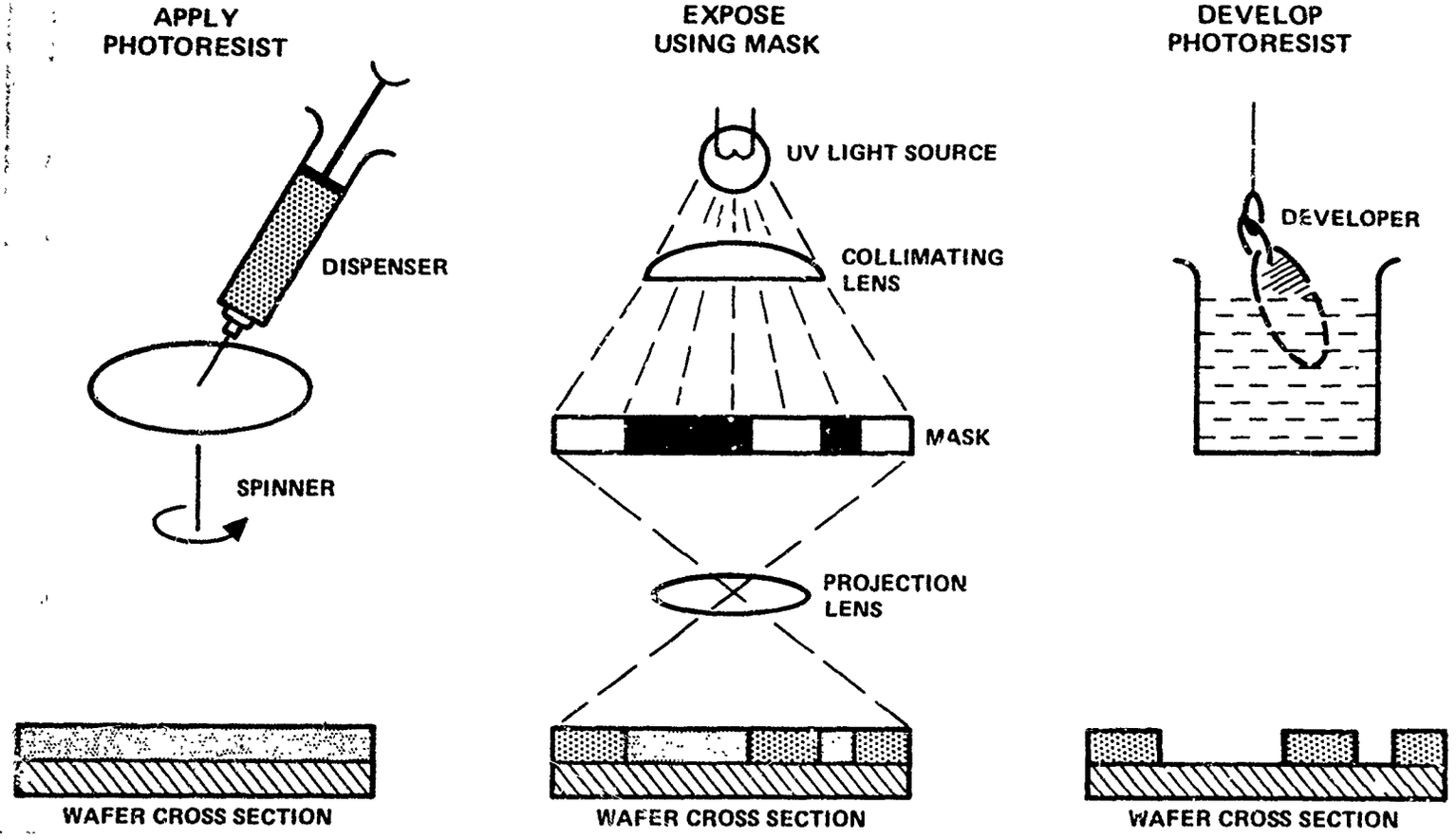


Figure B-1. Basic masking steps.

The transistors within the liquid crystal matrix structure are of the p-channel metal-oxide semiconductor (P-MOS) type. The basic steps required to build a P-MOS transistor, as illustrated in Figure B-2, are: (1) oxidizing the surface of the silicon wafer to form the field oxide; (2) masking and selective etching of the field oxide; (3) doping of the n-type silicon through the holes in the oxide to form regions of p-type silicon; (4) masking and stripping away the oxide in the region that is to become the gate of the transistor; (5) additional oxidizing of the silicon for a precise period of time to grow a thin oxide; (6) masking and stripping away part of the oxide so that contact may be made to the underlying p-regions; (7) depositing a conductive metal layer (polysilicon); and (8) masking and etching the conductive metal to define the gate region and the electrical contacts to the p-regions. The end product is a p-channel enhancement mode MOS transistor.

To turn the transistor ON, a voltage that is negative with respect to the substrate is applied to the gate, which drives electrons away from the region under the gate making it equivalent to a p-type material. When the transistor is ON, this "p-channel" is the conductive path between the p-doped source and drain regions. In this manner, the addressing circuits for the liquid crystal display (row and column electrode busses, field effect transistor switches and elemental storage capacitors) are formed in and on the surface of the silicon chip.

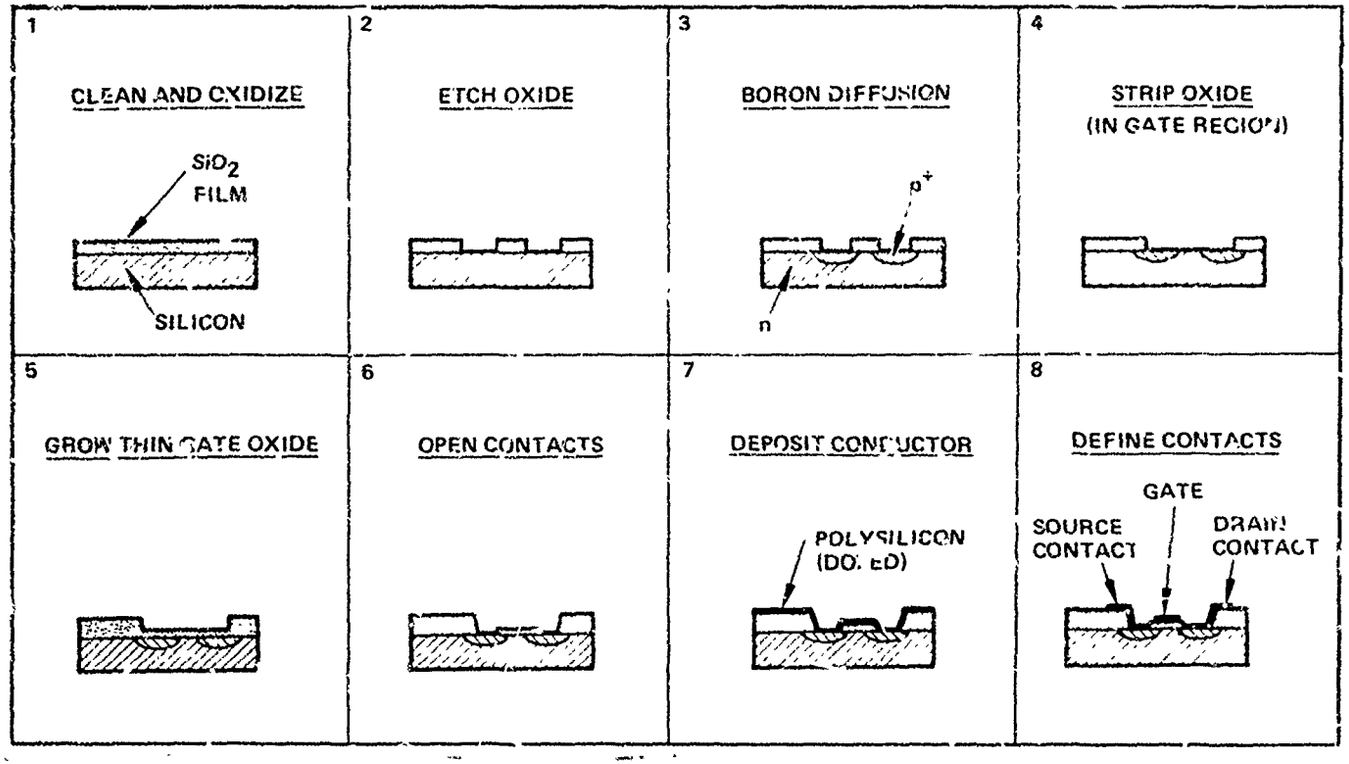


Figure B-2. MOS transistor fabrication.